

DM8203-E5/E6 Migration to DM8603

Application Note

CONFIDENTIAL

Hardware Change

1. Application schematic designs for DM8203-E5/E6 can interchange the DM8603 without any issues. The DM8603 is compatible in PIN assignment (PIN-to-PIN),. The one minor modification between the DM8203-E5/E6 and the DM8603 is to the bandgap resistance resistor. The only action is the replacement of the original 1.4K resistor with a 6.8K resistor. Any change to the PCB layout will not be required and no other modifications will need to be employed in migrating from the DM8203-E5/E6 to the DM8203E8.
2. PIN: TEST2

PIN No.	I/O	Description
59	I,PD	0: DM8203 Tie to GND in Application 1: DM8603 Tie to VCC3.3V

Hardware Additions

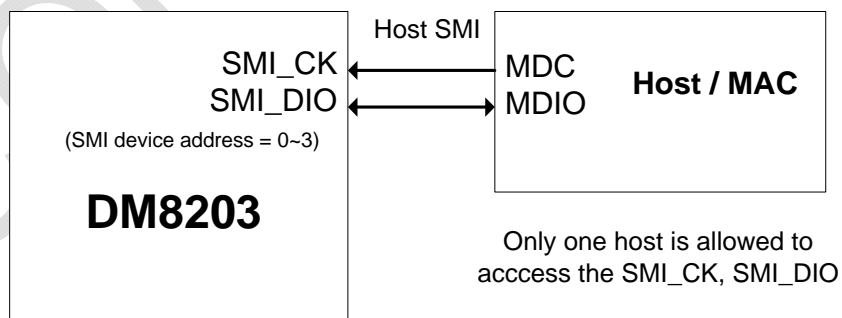
DM8203-E5/E6	DM8603
Fiber Mode Not Supported	Fiber Mode Internally Enabled (<i>Does Not Required the addition of a SD PIN</i>)
None	TXC2 output 50MHz clock in Reduce MII (RMII) mode
Strap PINs: [TXD2_3=1] & [TX2_2=1] - RESERVED	Strap PINs: [TXD2_3=1] & [TX2_2=1] - Enable P0, P1 Link Fault Pass-through (LFP) Function

Software Additions

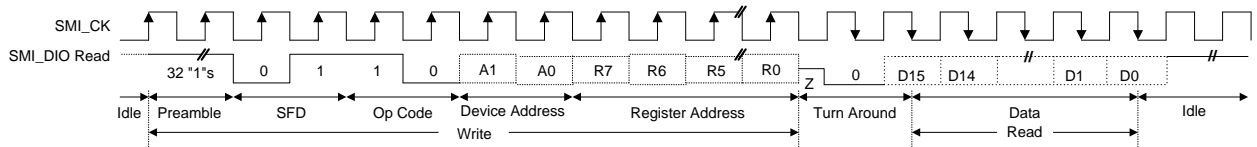
Function	DM8203-E5/E6	DM8603
Address Table Type	Unicast	Uni/Multi
Address Table Accessible	No	Yes
H/W IGMP-Snooping	No	Yes
MLD-Snooping	No	Yes
Unplug Clear Address	No	Yes
QinQ	No	Yes
STP/RSTP	No	Yes
Special Tag	No	Yes
SMI Format	See Note1	See Note2

Note1:

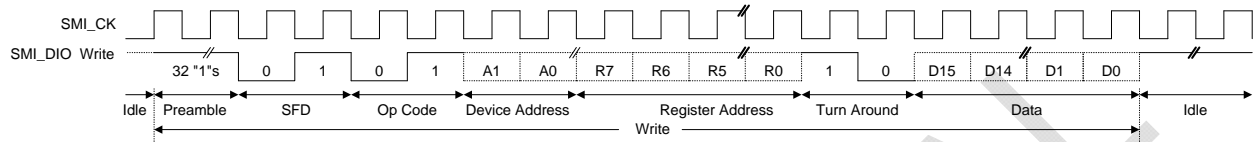
DM8203 Serial Management System (SMI FORMAT)



Host SMI - Read Frame Structure



Host SMI - Write Frame Structure

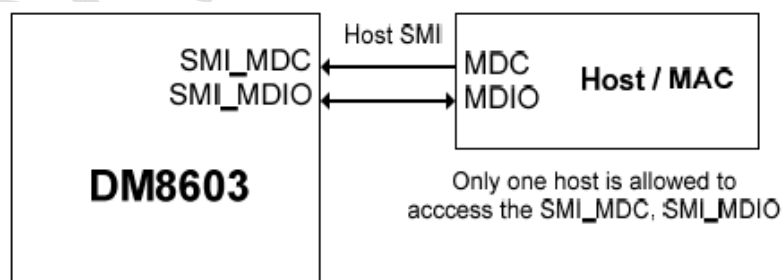


The Host SMI consists of two pins, one is SMI_CLK and another is SMI_DIO. User can access DM8203's EEPROM, PHY registers, MIB counters and Configuration registers through Host SMI.

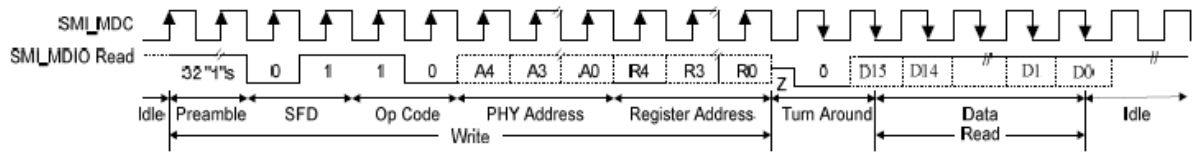
The <Device Address> field of the frame means SMI device address that is configured by strap pin (TXD2_0 & TXD2_1). The <Register Address> field of the frame is mapped to address of control and status register set of DM8203. The read/writ data is valid on low byte (D7~D0) of <Data> field, the high byte (D15~D8) of data is reserved.

Note1:

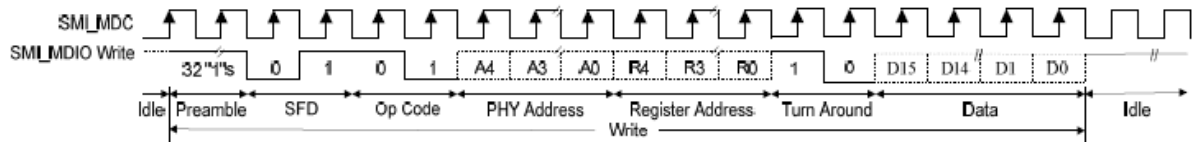
DM8603 Serial Management System (SMI FORMAT)



Host SMI - Read Frame Structure



Host SMI - Write Frame Structure



The Host SMI consists of two pins, one is SMI_MDC and another is SMI_MDIO. User can access DM8603's EEPROM, PHY registers, MIB counters and Configuration registers through Host SMI. The format is following. The <PHY Address> and <Register Address> fields of the frame are mapped to address of PHY register and Switch register set of DM8603.

Application Note Revision History

Date of Revision:
October 1, 2010

Revision Number:
00

Reason:
Originally Published
Application Note