

DM8203

Layout Guide

Version: 1.0

Version: DM8203-LG-V1.0
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• **1.Placement, Signal and Trace Routing**

- Place the 10/100M magnetic as closely as possible to the DM8203 and to the RJ-45 connector.
- Place the termination resistors 50Ω closely to the 10/100M magnetic and the DM8203 RX± pins and TX± pins. The 50Ω resistors and grounding capacitors of TX± and RX± should be placed near DM8203.
- The 25MHz crystal should not be placed near important signal traces, such as RX± receive pair and TX±transmit pair, band gap resistor, magnetic and board edge.
- Traces routed from the DM8203 RX± pair to the 10/100M magnetic and the RJ45 connector should run symmetrically, directly, identically, and closely. The same rule is applied to traces routed from the DM8203 TX± pair.

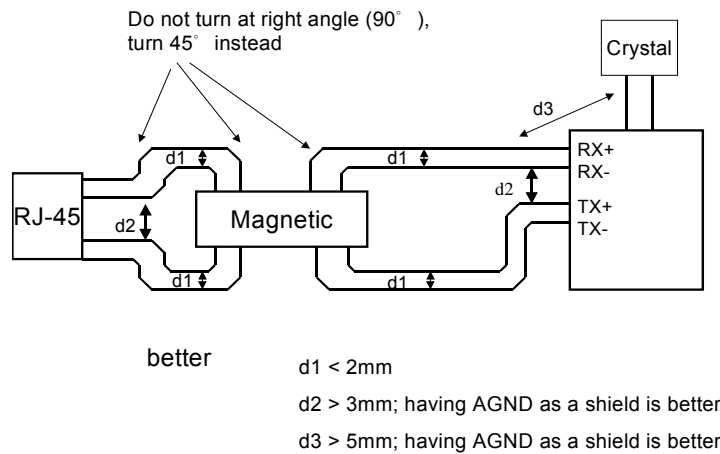


Fig.1-1 Better example for signal and trace routing

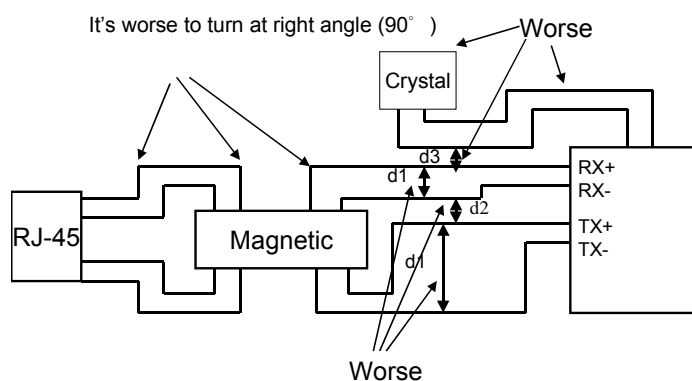


Fig.1-2 Worse example for signal and trace routing

- It is recommended that RX± receive and TX± transmit traces turn at 45° angle. Do not turn at right angle.

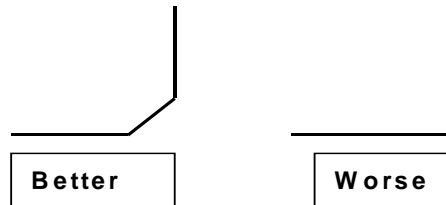


Fig.1-3 Examples for better trace and worse trace

- Avoid using vias in routing the traces of RX± pair and TX± pair.
- The RX± pair and TX± pair should be routed to have differential characteristic impedance of 100 Ohm. The clock should be routed to have characteristic impedance of 50 Ohm.
- Do not place the DM8203 RX± pair across the TX± pair. Keep the receive pair away from the transmit pair (no less than 3mm). It's better to place ground plane between these two pairs of traces.
- The network interface (see **Figure 1-1** and **Figure 1-2**) does not route any digital signal between the DM8203 RX± and TX± pairs to the RJ-45. Keep the two pairs away from all the other active signals and the chassis ground.
- It should be no power or ground plane in the area under the network side of the 10/100M magnetic and the area under the RJ-45 connector.
- Any terminated pins of the RJ-45 connector and the magnetic (see **Figure 1-1** and **Figure 1-2**) should be tied as closely as possible to the chassis ground through a resistor divider network 75Ω resistors (no more than 2mm to the magnetic) and a 0.01μF/2KV bypass capacitor.
- The Band Gap resistor should be placed as close as possible to pins 47 and 48 (BGRES, BGRESG) (no more than 3mm). Avoid running any high-speed signal near the Band Gap resistor placement (no less than 3mm from 25MHz X1 and X2).

2. DM8203 10Base-T/100Base-TX Application

2-1. DM8203 Application

Fig. 2-1-1 illustrates the two types of the specific magnetic interconnect and how to connect with DM8203. These magnetics are not pin-to-pin compatible. It must be considered when using the DM8203 in auto-MDIX mode.

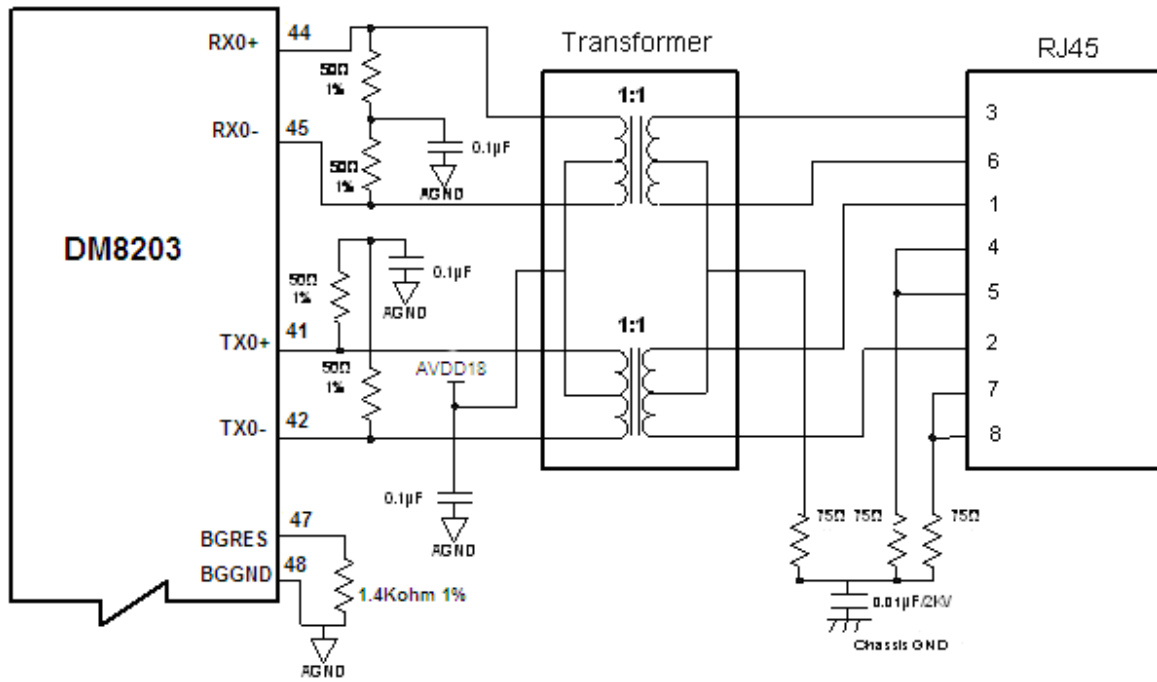
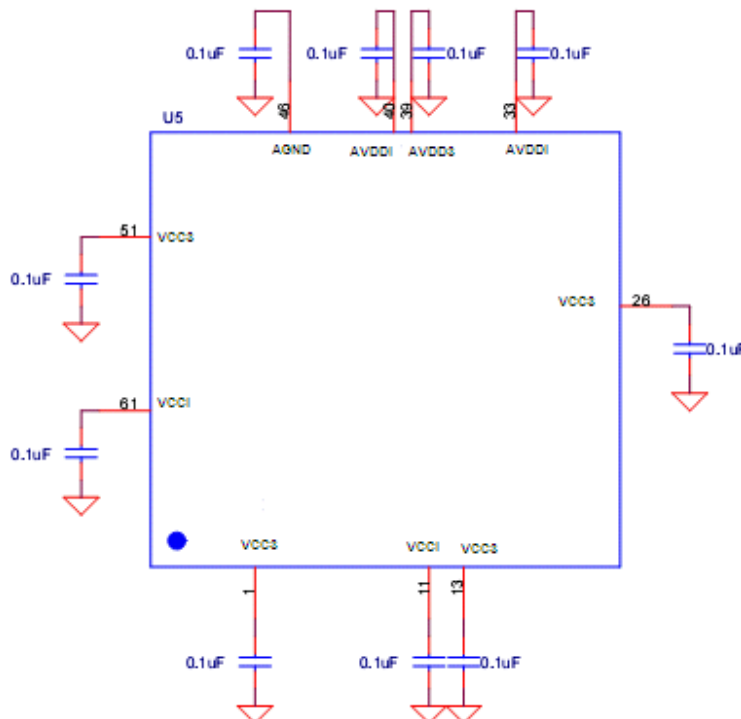


Fig. 2-1-1 Application with auto-MDIX transformer (turn ratio 1CT: 1CT)

3. Power Supply Decoupling Capacitors

- Place all the decoupling capacitors for all power supply pins as closely as possible to the power pads of the DM8203 (no more than 2.5mm from the above mentioned pins). The recommended decoupling capacitor is 0.1 μ F or 0.01 μ F.
- The PCB layout and power supply decoupling should provide sufficient decoupling to achieve the following when measured at the device:
 - (1) All VCC3/VCCIs and AVDD3/AVDDIs should be within 50mVpp of each other,
 - (2) All DGNDs and AGNDs should be within 50mVpp of each other.
 - (3) The resultant AC noise voltage measured across each VCC3/VCCI/DGND set and AVDD3/AVDDI/AGND set should be less than AVDDI.
- The 0.1-0.01 μ F decoupling capacitor should be connected between each VCC3/VCCI/DGND set and AVDD3/AVDDI/AGND set and be placed as closely as possible to the pins of DM8203. The conservative approach is to use two decoupling capacitors on each VCC3/VCCI/DGND set and AVDD3/AVDDI/AGND set. One 0.1 μ F is for low frequency noise, and the other 0.01 μ F is for high frequency noise on the power supply.
- The AVDD3/AVDDI connection to the transmit center tap of the magnetic has to be well decoupled to minimize common mode noise injection from the power supply into the twisted pair cable. It is recommended that a 0.01 μ F decoupling capacitor be placed between the center tap AVDD3/AVDDI to AGND ground plane.



This decoupling capacitor should be placed as closely as possible to the center tap of the magnetic. One 220 μ F Capacitor should be connected between each AVDD3/AVDDI and AGND. Please see the **Fig.3-1**.

Fig. 3-1 the decoupling capacitors for the ground pins of DM8203

4. Ground Plane Layout

- Place a single ground plane approach to minimize EMI. Ground plane partitioning may cause increased EMI emissions that could make the network interface circuit not comply with specific FCC part 15 and CE regulations.
- The ground plane needs to be divided into analog ground domain and digital ground domain, The connection of these two domain should be far away from the AGND pins of DM8203 (see **Fig. 4-1**).
- All AGND pins could not directly short each other (see **Fig.4-2**). They must be directly connected to the analog ground domain.
- Analog ground domain area should be as large as possible

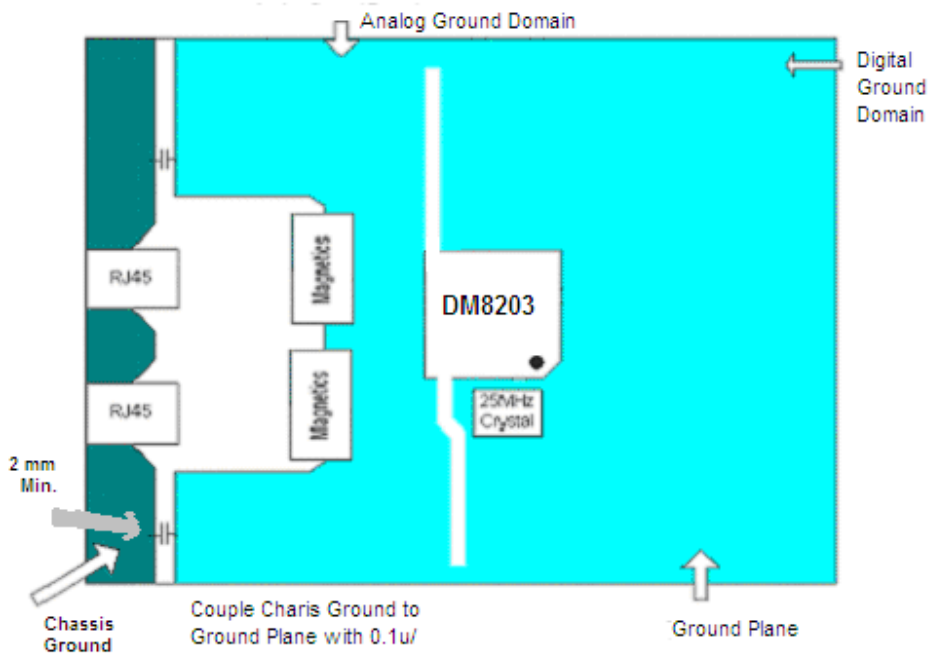


Fig.4-1 Ground plane separation for DM8203

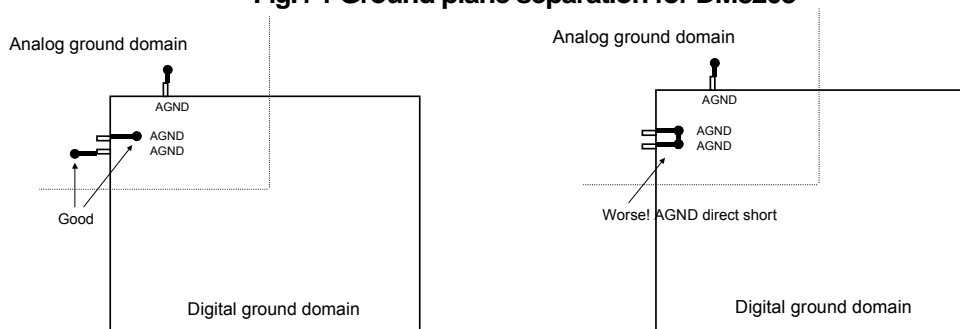


Fig.4-2 All AGND pins must be directly connected to analog ground

5. Power Plane Partitioning

- The power planes should be approximately illustrated in **Fig. 5-1**.
- The analog power plane should be separated from the noisy digital (logic) power plane.

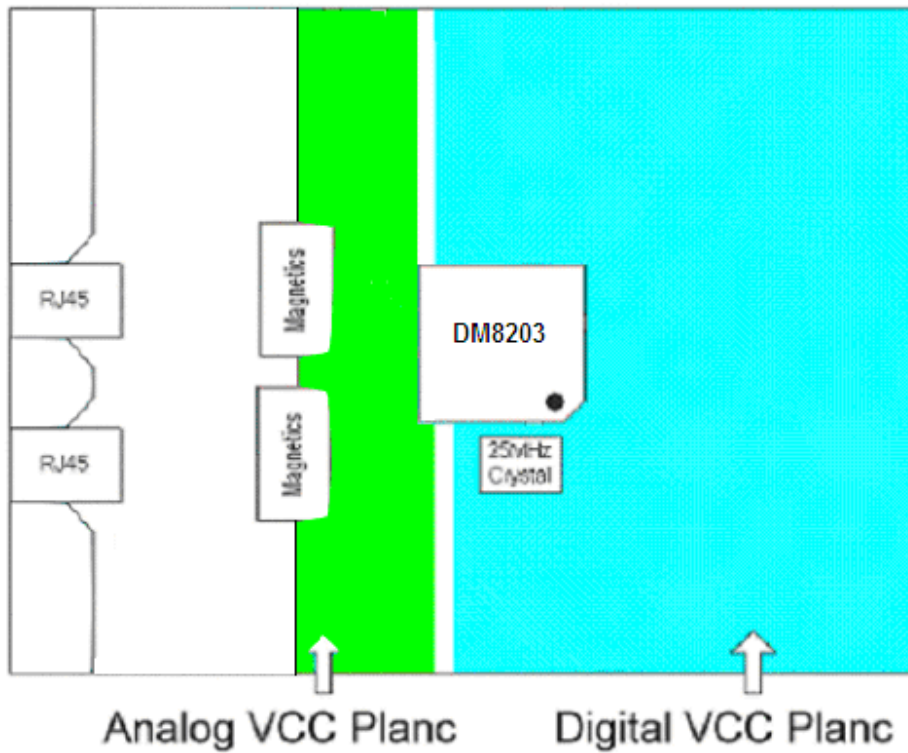


Fig. 5-1 Power planes partitioning for DM8203

6. Magnetic Selection Guide

- Refer to the following **tables 6-1 and 6-2** for 10/100M magnetic sources and specification requirements. The magnetics which meet these requirements are available from a variety of magnetics manufacturers. Designers should test and qualify all magnetic specifications before using them in an application. The magnetic listed in the following table are electrically equivalent, but may not be pin-to-pin compatible.

Manufacturer	Part Number
Pulse Engineering	PE-68515, H1102
YCL	PH163112, PH163539
DELTA	LFE8505T , LFE8563T, LFE8583
GTS	FC-618SM
MACOM	HS9016, HS9024

Table 6-1: 10/100M Magnetic Sources

Parameter	Values	Units	Test Condition
Tx / RX turns ratio	1:1 CT / 1:1	-	-
Inductance	350	μH (Min)	-
Insertion loss	1.1	DB (Max)	1 – 100 MHz
Return loss	-18	DB (Min)	1 –30 MHz
	-14	DB (Min)	30 – 60 MHz
	-12	DB (Min)	60 – 80 MHz
Differential to common mode rejection	-40	DB (Min)	1 – 60 MHz
	-30	DB (Min)	60 – 100 MHz
Transformer isolation	1500	V	-

Table 6-2: Magnetic Specification Requirements

7. Crystal Selection Guidelines

- A crystal can be used to generate the 25.000MHz reference clock instead of an oscillator. The crystal must be a fundamental type, series-resonant, connect to X1 and X2, and shunt each crystal lead to ground with a 22pF capacitor as shown in **Fig.7-1**.

PARAMETER	SPEC
Type	Fundamental, series-resonant
Frequency	25.000 MHz +/- 30ppm
Equivalent Series Resistance	25 ohms max
Load Capacitance	22 pF typ.
Case Capacitance	7 pF max.
Power Dissipation	1mW max.

Table 7-1: Crystal Specifications

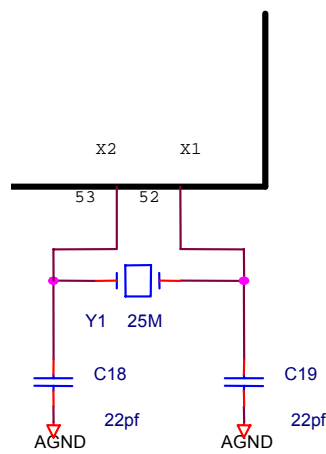


Fig. 7-1 Crystal circuit for DM8203

8. Layout Tracing Notes for MII Signals of DM8203 to external PHY

- The length of the trace routing for the Media Independent Interface (MII) signals should be as short and direct as possible between the DM8203 and external PHY (maximum trace distance should be shorter than 20cm). These MII signals are as follows,

CRS2, COL2, TXD2_3, TXD2_2, TXD2_1, TXD2_0, TXE2, TXC2, TXER2
RXER2, RXC2, RXDV2, RXD2_0, RXD2_1, RXD2_2, RXD2_3, MDC, MDIO

- TXD2_[0-3] and TXC2 length mismatch should be within 2cm.
- RXD2_[0-3] and RXC2 length mismatch should be within 2cm.
- All signal traces should be considered to have characteristic impedance of 50 Ohm.