



DM8203I

Industrial-Temperature 10/100 Mbps 3 - port Ethernet Switch Controller With MII / RMI Interface

DAVICOM Semiconductor, Inc.

DM8203I

Industrial-Temperature 10/100 Mbps 3-port Ethernet
Switch Controller with MII / RMI Interface

DATASHEET

Preliminary Datasheet
Version: DM8203I-DS-P01
August 20, 2010

CONTENT

| | |
|---|-----------|
| 1. GENERAL DESCRIPTION..... | 9 |
| 2. BLOCK DIAGRAM..... | 9 |
| 3. FEATURES | 10 |
| 4. PIN CONFIGURATION | 11 |
| 5. PIN DESCRIPTION | 12 |
| 5.1 P2 MII / RMI / Reverse MII Interfaces..... | 12 |
| 5.1.1 MII Interfaces | 12 |
| 5.1.2 RMI Interfaces | 12 |
| 5.1.3 Reverse MII Interfaces | 13 |
| 5.2 EEPROM Interfaces..... | 13 |
| 5.3 LED Pins..... | 13 |
| 5.4 Clock Interface..... | 14 |
| 5.5 Network Interface..... | 14 |
| 5.6 Miscellaneous Pins..... | 14 |
| 5.7 Power Pins..... | 14 |
| 5.8 Strap pins table..... | 15 |
| 6. CONTROL AND STATUS REGISTER SET..... | 16 |
| 6.1 EEPROM Control Register (0AH)..... | 17 |



| | |
|--|-----------|
| 6.2 EEPROM & PHY Control Register (0BH) | 18 |
| 6.3 EEPROM & PHY Address Register (0CH) | 18 |
| 6.4 EEPROM & PHY Data Register (0DH~0EH) | 18 |
| 6.5 Vendor ID Registers (28H~29H) | 18 |
| 6.6 Product ID Registers (2AH~2BH)..... | 18 |
| 6.7 Chip Revision Register (2CH) | 19 |
| 6.8 Port 2 driving capability Register (3AH)..... | 20 |
| 6.9 Port 2 MAC Control Register (3BH) | 20 |
| 6.10 PHY Control Register (3CH)..... | 20 |
| 6.11 PHY Control Test Register (3EH)..... | 20 |
| 6.12 Monitor Strap pin & enable pin status Register 1 (41H) | 21 |
| 6.13 Monitor Strap pin & enable pin status Register 2 (42H) | 21 |
| 6.14 Switch Control Register 1 (52H)..... | 21 |
| 6.15 VLAN Control Register 1 (53H)..... | 22 |
| 6.16 Switch Status Register (54H) | 22 |
| 6.17 Switch Control Register 2 (55H)..... | 22 |
| 6.18 VLAN Control Register 2 (56H)..... | 23 |
| 6.19 Per Port Control/Status Index Register (60H) | 23 |
| 6.20 Per Port Control Data Register (61H) | 23 |
| 6.21 Per Port Status Data Register (62H) | 24 |



6.22 Per Port Forward Control Register 1 (63H)..... 24

6.23 Per Port Forward Control Register 2 (64H)..... 25

6.24 Per Port Forward Control Register 3 (65H)..... 25

6.25 Per Port Ingress/Egress Control Register (66H)..... 26

6.26 Bandwidth Control Setting Register (67H) 27

6.27 Per Port Block Unicast ports Control Register (68H) 28

6.28 Per Port Block Multicast ports Control Register (69H)..... 28

6.29 Per Port Block Broadcast ports Control Register (6AH) 28

6.30 Per Port Block Unknown ports Control Register (6BH)..... 28

6.31 Per Port Priority & VLAN Control Register (6CH)..... 28

6.32 Per Port Priority Queue Control Register (6DH) 29

6.33 Per Port VLAN Tag Low Byte Register (6EH) 29

6.34 Per Port VLAN Tag High Byte Register (6FH) 29

6.35 MIB counters Port Index Register (80H)..... 30

6.36 MIB counter Data Register (81H~84H) 30

6.37 VLAN grouping table Registers (B0H~BFH)..... 31

6.38 TOS Priority Map Registers (C0H~CFH) 34

6.39 VLAN Priority Map Registers (D0H~D1H) 37

6.40 Memory Access Enable Register (F0H) 38

6.41 Memory Low Address Register (F1H)..... 38



6.42 Memory High Address Register (F2H)..... 38

6.43 Memory Dummy Read Data Register (F3H)..... 38

6.44 Memory Read Data Register (F4H) 38

6.45 Memory Write Data Register (F5H) 38

6.46 Memory Write Bits7~0 Data Register (F6H)..... 38

6.47 Memory Write Bits15~8 Data Register (F7H)..... 38

7. EEPROM FORMAT..... 39

8. PHY REGISTERS 42

8.1 Basic Mode Control Register (BMCR) – 00H 43

8.2 Basic Mode Status Register (BMSR) – 01H 44

8.3 PHY ID Identifier Register #1 (PHYID1) – 02H..... 45

8.4 PHY ID Identifier Register #2 (PHYID2) – 03H..... 45

8.5 Auto-negotiation Advertisement Register (ANAR) – 04H 46

8.6 Auto-negotiation Link Partner Ability Register (ANLPAR) – 05H..... 47

8.7 Auto-negotiation Expansion Register (ANER) - 06H..... 48

8.8 DAVICOM Specified Configuration Register (DSCR) – 10H..... 48

8.9 DAVICOM Specified Configuration and Status Register (DSCSR) – 11H..... 50

8.10 10BASE-T Configuration/Status (10BTCSR) – 12H..... 51

8.11 Power down Control Register (PWDOR) – 13H..... 51

8.12 (Specified config) Register – 14H 52



8.13 DAVICOM Specified Receive Error Counter Register (RECR) – 16H..... 53

8.14 DAVICOM Specified Disconnect Counter Register (DISCR) – 17H..... 53

8.15 Power Saving Control Register (PSCR) – 1DH..... 53

9. FUNCTIONAL DESCRIPTION..... 54

9.1 Serial Management Interface 54

9.2 Switch function: 55

 9.2.1 Address Learning 55

 9.2.2 Address Aging 55

 9.2.3 Packet Forwarding 55

 9.2.4 Inter-Packet Gap (IPG)..... 55

 9.2.5 Back-off Algorithm..... 55

 9.2.6 Late Collision 55

 9.2.7 Full Duplex Flow Control 55

 9.2.8 Half Duplex Flow Control 55

 9.2.9 Partition Mode..... 56

 9.2.10 Broadcast Storm Filtering 56

 9.2.11 Bandwidth Control..... 56

 9.2.12 Port Monitoring Support..... 56

 9.2.13 VLAN Support..... 57

 9.2.13.1 Port-Based VLAN 57

 9.2.13.2 802.1Q-Based VLAN..... 57

 9.2.13.3 Tag/Untag 57

 9.2.14 Priority Support..... 58

 9.2.14.1 Port-Based Priority 58

 9.2.14.2 802.1p-Based Priority..... 58

 9.2.14.3 DiffServ-Based Priority..... 58

9.3 MII Interface..... 59

 9.3.1 MII data interface..... 59

 9.3.2 MII Serial Management 59



9.3.3 Serial Management Interface 60

9.3.4 Management Interface - Read Frame Structure..... 60

9.3.5 Management Interface - Write Frame Structure..... 60

9.4 Internal PHY functions 61

9.4.1 100Base-TX Operation..... 61

9.4.1.1 4B5B Encoder 61

9.4.1.2 Scrambler..... 61

9.4.1.3 Parallel to Serial Converter 61

9.4.1.4 NRZ to NRZI Encoder 61

9.4.1.5 MLT-3 Converter 61

9.4.1.6 MLT-3 Driver..... 61

9.4.1.7 4B5B Code Group 62

9.4.2 100Base-TX Receiver 63

9.4.2.1 Signal Detect 63

9.4.2.2 Adaptive Equalization..... 63

9.4.2.3 MLT-3 to NRZI Decoder..... 63

9.4.2.4 Clock Recovery Module..... 63

9.4.2.5 NRZI to NRZ..... 63

9.4.2.6 Serial to Parallel..... 63

9.4.2.7 Descrambler 63

9.4.2.8 Code Group Alignment..... 64

9.4.2.9 4B5B Decoder 64

9.4.3 10Base-T Operation 64

9.4.4 Collision Detection 64

9.4.5 Carrier Sense..... 64

9.4.6 Auto-Negotiation..... 64

9.5 HP Auto-MDIX Functional Descriptions 64

10. DC AND AC ELECTRICAL CHARACTERISTICS 66

10.1 Absolute Maximum Ratings 66

10.2 Operating Conditions 66



| | |
|--|-----------|
| 10.3 DC Electrical Characteristics | 67 |
| 10.4 AC characteristics..... | 67 |
| 10.4.1 Power On Reset Timing..... | 67 |
| 10.4.2 Port 2 MII Interface Transmit Timing..... | 68 |
| 10.4.3 Port 2 MII Interface Receive Timing..... | 68 |
| 10.4.4 MII Management or host SMI Interface Timing | 69 |
| 10.4.5 EEPROM timing | 70 |
| 11. APPLICATION CIRCUIT | 71 |
| 11.1 Main circuit..... | 71 |
| 11.2 Application of Reverse MII..... | 72 |
| 12. PACKAGE INFORMATION..... | 73 |
| 13. ORDERING INFORMATION | 74 |

1. General Description

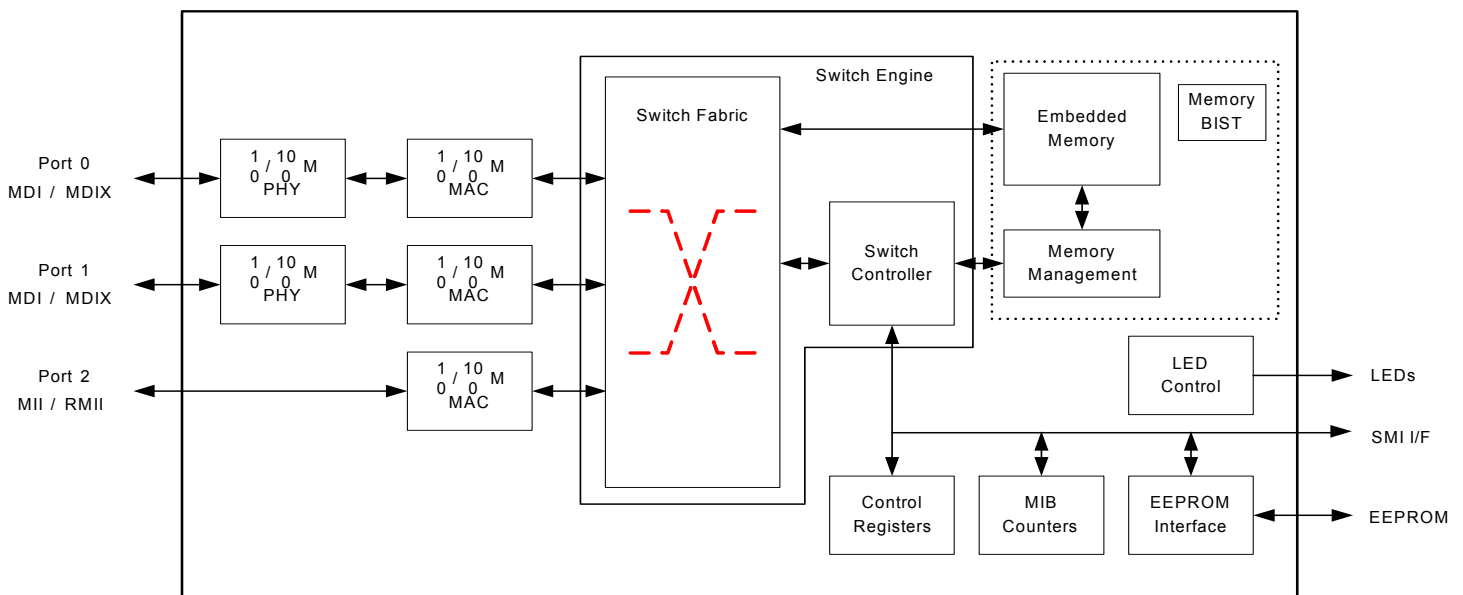
The DM8203I is Davicom's new fully integrated industrial-temperature three-port 10M/100Mbps Fast Ethernet Controller. As a fast Ethernet switch, the DM8203I consists of two PHY ports and a third port with either MII or RMII interface. As the DM8203I was designed with our customers' requirements in mind, the switch is optimized for high performance while being highly cost-effective. The DM8203I has also been design and tested to withstand the rigors of an industrial environment.

The two PHY ports on the DM8203I are IEEE 802.3u standards compliant. Aside for the first two PHY ports and in an effort for maximum application flexibility, the third port on the DM8203I offers the options to either connect with an Ethernet PHY, reversed MII, or RMII. The reversed MII configuration is used to connect with SoC's with a MII interface. The RMII interface is the alternative interface configuration in case of the need to connect a lower pin count Ethernet PHY or SoC.

To maximize the performance of each port, the DM8203I was designed with a number of features. For proper bandwidth, each port also supports ingress and/or egress rate control. In support of efficient packet forwarding, the DM8203I has port-based VLAN with tag/un-tag functions for up to 16 groups of 802.1Q. Each port includes MIB counters, loop-back capability, built in memory self test (BIST) for the system, and board level diagnostic.

In designing for the requirements of various data, voice, and video applications, enough internal memory has been provided for usage of the DM8203I's three ports, and the internal memory supports up to 1K uni-cast MAC address table. Then to meet the demands of various bandwidth and latency issues in data, voice, and video applications, each port of the DM8203I has four priority transmit queues. These queues can be defined either through port-based operation, 802.1p VLAN, or the IP packet TOS field automatically.

2. Block Diagram

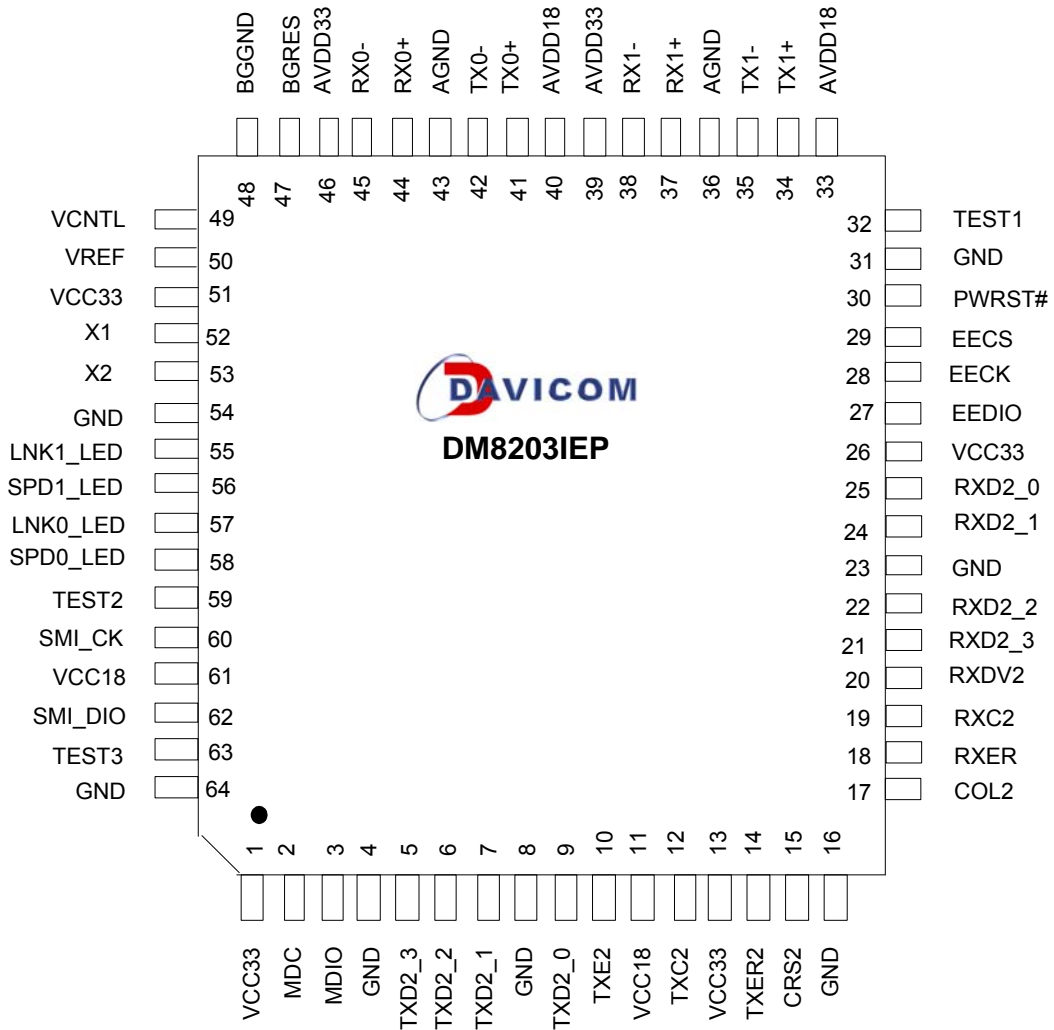


3. Features

- IEEE 802.3 10Base-T/100Base-TX compatible
- Ethernet Switch Ports:
 - Two 10/100Mbps PHY
 - One MII/RMII interface with Reversed - MII support
- Supports auto crossover function - HP Auto-MDIX
- Flow Control
 - Supports IEEE 802.3x Flow Control in Full-duplex mode
 - Supports Back Pressure Flow Control in Half-duplex mode
- Per port support bandwidth, ingress and egress rate control
- Per port support priority queues
 - Each port with four queues
 - Port-based, 802.1P VLAN, or IP TOS priority
- Supports 802.1Q VLAN for up-to 16 VLAN groups
- Supports VLAN ID tag/untag options
- Supports up-to 1K Uni-cast MAC addresses
- Supports store and forward switching approach
- Supports Broadcast Storming filter function
- Supports Serial Data Management Interface
- Automatic aging scheme
- Supports MIB counters for diagnostic
- Supports LFP (Link Fault Pass-through)
- EEPROM Interface
 - power up configurations
 - 93C46 or 93C56 auto detection
- Package
 - 64-pin LQFP
- Temperature
 - Supports Industrial-temperature: -40 °C~ +85°C
- Power
 - 1.8V/3.3V Dual Power
 - 3.3V I/O with 5V tolerance

4. Pin Configuration

64 pin LQFP:



5. Pin Description

I = Input, O = Output, I/O = Input / Output, O/D = Open Drain, P = Power, PD=internal pull-low (about 50K Ohm)
= asserted Low

5.1 P2 MII / RMII / Reverse MII Interfaces

5.1.1 MII Interfaces

| Pin No. | Pin Name | I/O | Description |
|-------------|----------|------|---|
| 2 | MDC | O,PD | MII Serial Management Data Clock |
| 3 | MDIO | I/O | MII Serial Management Data |
| 5,6,7,9 | TXD2_3~0 | O,PD | Port 2 MII Transmit Data 4-bit nibble data outputs (synchronous to the TXC2) |
| 10 | TXE2 | O,PD | Port 2 MII Transmit Enable |
| 12 | TXC2 | I/O | Port 2 MII Transmit Clock. |
| 14 | TXER2 | O,PD | Port 2 MII Transmit Error |
| 15 | CRS2 | I/O | Port 2 MII Carrier Sense |
| 17 | COL2 | I/O | Port 2 MII Collision Detect. |
| 18 | RXER2 | I | Port 2 MII Receive Error |
| 19 | RXC2 | I | Port 2 MII Receive Clock |
| 20 | RXDV2 | I | Port 2 MII Receive Data Valid |
| 21,22,24,25 | RXD2_3~0 | I | Port 2 MII Receive Data 4-bit nibble data input (synchronous to RXC2) |

5.1.2 RMII Interfaces

| Pin No. | Pin Name | I/O | Description |
|---------|----------|------|----------------------------------|
| 2 | MDC | O,PD | MII Serial Management Data Clock |
| 3 | MDIO | I/O | MII Serial Management Data |
| 5,6 | TXD2_3~2 | O,PD | Reserved |
| 7,9 | TXD2_1~0 | O,PD | RMII Transmit Data |
| 10 | TXE2 | O,PD | RMII Transmit Enable. |
| 12 | TXC2 | O | Output 50MHz clock |
| 14 | TXER2 | O | Port 2 MII Transmit Error |
| 15 | CRS2 | I | RMII CRS_DV |
| 17 | COL2 | I | Reserved. |
| 18 | RXER2 | I | Reserved |
| 19 | RXC2 | I | 50MHz reference clock. |
| 20 | RXDV2 | I | Reserved |
| 21,22 | RXD2_3~2 | I | Reserved |
| 24,25 | RXD2_1~0 | I | RMII Receive Data. |

5.1.3 Reverse MII Interfaces

| Pin No. | Pin Name | I/O | Description |
|-------------|----------|------|---|
| 2 | MDC | O,PD | Reserved |
| 3 | MDIO | I/O | Reserved |
| 5,6,7,9 | TXD2_3~0 | O,PD | Port 2 MII Transmit Data 4-bit nibble data outputs (synchronous to the TXC2) |
| 10 | TXE2 | O,PD | Port 2 MII Transmit Enable |
| 12 | TXC2 | O | 25MHz clock output |
| 14 | TXER2 | O,PD | Port 2 MII Transmit Error |
| 15 | CRS2 | O | Port 2 carrier sense output when TXE2 or RXDV2 asserted. |
| 17 | COL2 | O | Port 2 collision output when TXE2 and RXDV2 asserted. |
| 18 | RXER2 | I | Port 2 MII Receive Error |
| 19 | RXC2 | I | Port 2 MII Receive Clock |
| 20 | RXDV2 | I | Port 2 MII Receive Data Valid |
| 21,22,24,25 | RXD2_3~0 | I | Port 2 MII Receive Data 4-bit nibble data input (synchronous to RXC2) |

5.2 EEPROM Interfaces

| Pin No. | Pin Name | I/O | Description |
|---------|----------|------|--|
| 27 | EEDIO | I/O | EEPROM Data In/Out |
| 28 | EECK | O,PD | EEPROM Serial Clock This pin is used as the clock for the EEPROM data transfer. |
| 29 | EECS | O,PD | EEPROM Chip Selection. |

5.3 LED Pins

| Pin No. | Pin Name | I/O | Description |
|---------|----------|-----|--|
| 55 | LNK1_LED | O | Port 1 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY1 |
| 56 | SPD1_LED | O | Port 1 Speed LED Its low output indicates that the internal PHY1 is operated in 100M/S, or it is floating for the 10M mode of the internal PHY1 |
| 57 | LNK0_LED | O | Port 0 Link / Active LED It is the combined LED of link and carrier sense signal of the internal PHY0 |
| 58 | SPD0_LED | O | Port 0 Speed LED Its low output indicates that the internal PHY0 is operated in 100M/S, or it is floating for the 10M mode of the internal PHY0 |

5.4 Clock Interface

| Pin No. | Pin Name | I/O | Description |
|---------|----------|-----|-------------------|
| 52 | X1 | I | Crystal 25MHz In |
| 53 | X2 | O | Crystal 25MHz Out |

5.5 Network Interface

| Pin No. | Pin Name | I/O | Description |
|---------|----------|-----|---|
| 34,35 | TX1+/- | I/O | Port 1 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode. |
| 37,38 | RX1+/- | I/O | Port 1 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode. |
| 41,42 | TX0+/- | I/O | Port 0 TP TX These two pins are the Twisted Pair transmit in MDI mode or receive in MDIX mode. |
| 44,45 | RX0+/- | I/O | Port 0 TP RX These two pins are the Twisted Pair receive in MDI mode or transmit in MDIX mode. |
| 47 | BGRES | I/O | Band gap Pin Connect a 6.8K resistor to BGGND in application. |
| 48 | BGGND | P | Band gap Ground |
| 49 | VCNTL | I/O | 1.8V Voltage control |
| 50 | VREF | O | Voltage Reference Connect a 0.1u capacitor to ground in application. |

5.6 Miscellaneous Pins

| Pin No. | Pin Name | I/O | Description |
|---------|----------|------|---|
| 30 | PWRST# | I | Power on Reset Low active with minimum 1ms |
| 60 | SMI_CK | I | Serial data management interface clock |
| 62 | SMI_DIO | I/O | Serial data management interface in / out |
| 32 | TEST1 | I,PD | Tie to VCC3 in application |
| 59 | TEST2 | I,PD | Tie to GND in application |
| 63 | TEST3 | I,PD | Tie to VCC3 in application |

5.7 Power Pins

| Pin No. | Pin Name | I/O | Description |
|--------------------|----------|-----|--------------------------|
| 1,13,26,51 | VCC33 | P | Digital 3.3V |
| 11,61 | VCC18 | P | Internal 1.8V core power |
| 4,8,16,23,31,54,64 | GND | P | Digital GND |
| 39,46 | AVDD33 | P | Analog 3.3V power |
| 33,40 | AVDD18 | P | Analog 1.8V power |
| 36,43 | AGND | P | Analog GND |

5.8 Strap pins table

1: pull-high 1K~10K, 0: floating (default).

| Pin No. | Pin Name | Description |
|---------|----------|--|
| 28 | EECK | 0: Port 2 in force 10 Mbps mode 1: Port 2 in force 100 Mbps mode |
| 29 | EECS | 0: Port 0 is TP mode 1: Port 0 is Fiber mode |
| 14 | TXER2 | 0: Port 1 is TP mode 1: Port 1 is Fiber mode |
| 2 | MDC | 0: BIST 1: Bypass BIST |
| 5 | TXD2_3 | TXD2_3 TXD2_2 Mode |
| 6 | TXD2_2 | 0 0 Port 2 MII mode |
| | | 0 1 Port 2 Reverse MII mode |
| | | 1 0 Port 2 RMII mode |
| | | 1 1 Enable P0,P1 LFP function (P2 in MII mode) |
| 7,9 | TXD2_1,0 | SMI device address 1,0 TXD2_1 TXD2_0 0 0 : Device address 0 0 1 : Device address 1 1 0 : Device address 2 1 1 : Device address 3 |
| 10 | TXE2 | 0: Port 2 normal mode 1: Port 2 force mode |

6. Control and Status Register Set

The DM8203I implements several control and status registers, which can be accessed by the serial management interface. These CSRs are byte aligned. All CSRs are set to their default values by hardware or software reset unless specified

| Register | Description | Offset | Default value after reset |
|----------------|---|---------|---------------------------|
| ECR | EEPROM Control Register | 0AH | 00H |
| EPCR | EEPROM & PHY Control Register | 0BH | 00H |
| EPAR | EEPROM & PHY Address Register | 0CH | 40H |
| EPDRL | EEPROM & PHY Low Byte Data Register | 0DH | XXH |
| EPDRH | EEPROM & PHY High Byte Data Register | 0EH | XXH |
| VID | Vendor ID | 28H-29H | 0A46H |
| PID | Product ID | 2AH-2BH | 8203H |
| CHIPR | CHIP Revision Registers | 2CH | 03H |
| SMI_CNTRL | Serial Bus Err Control Register | 36H | 00H |
| SMI_STATU S | Serial Bus Status Check Register | 37H | 00H |
| P2FRV | Port 2 driving capability Register | 3AH | 20H |
| P2_CNTRL | Port 2 MAC Control | 3BH | 00H |
| PHY_CTL | PHY Control | 3CH | 00H |
| PHY_BIAS | PHY TX Bias Control Test | 3EH | 03H |
| DEBUG | Debug Control Register | 3FH | 00H |
| MONI_CNTR L | Monitor Control Register | 40H | |
| MONIR1 | Monitor Register 1 | 41H | |
| MONIR2 | Monitor Register 2 | 42H | |
| G_RX_BUF | Global RX Buffer used Counter | 44H | 00H |
| P0_RX_BUF | Port0 RX Buffer used Counter | 45H | 00H |
| P1_RX_BUF | Port1 RX Buffer used Counter | 46H | 00H |
| P2_RX_BUF | Port2 RX Buffer used Counter | 47H | 00H |
| SWITCHCR1 | SWITCH Control Register 1 | 52H | 00H |
| VLANCR 1 | VLAN Control Register 1 | 53H | 00H |
| SWITCHSR | SWITCH Status Register | 54H | 00H |
| SWITCHCR2 | SWITCH Control Register 2 | 55H | |
| VLANCR 2 | VLAN Control Register 2 | 56H | |
| DSP1,2 | DSP Control Register I,II | 58H~59H | 0000H |
| P_INDEX | Per Port Control/Status Index Register | 60H | 00H |
| P_CTRL | Per Port Control Data Register | 61H | 00H |
| P_STUS | Per Port Status Data Register | 62H | 00H |
| P_FORW1 | Per Port Forward Register 1 | 63H | |
| P_FORW2 | Per Port Forward Register 2 | 64H | |
| P_FORW3 | Per Port Forward Register 3 | 65H | |
| P_RATE | Per Port Ingress and Egress Rate Register | 66H | 00H |
| P_BW | Per Port Bandwidth Control Register | 67H | 00H |
| P_UNICAST | Per Port Block Unicast ports Register | 68H | 00H |
| P_MULTI | Per Port Block Multicast ports Register | 69H | 00H |
| P_BCAST | Per Port Block Broadcast ports Register | 6AH | 00H |



| | | | |
|------------|---|---------|---------|
| P_UNKNWN | Per Port Block Unknown ports Register | 6BH | 00H |
| P_PRI_VLAN | Per Port Priority & VLAN Control Register | 6CH | |
| P_PRI | Per Port Priority Queue Register | 6DH | 00H |
| VLAN_TAGL | Per Port VLAN Tag Low Byte Register | 6EH | 01H |
| VLAN_TAGH | Per Port VLAN Tag High Byte Register | 6FH | 00H |
| P_BUF_MAN | Per Port Buffer Management Register 1~4 | 70H~73H | |
| P_MIB_IDX | Per Port MIB counter Index Register | 80H | 00H |
| MIB_DAT | MIB counter Data Register bit 0~7 | 81H | 00H |
| MIB_DAT | MIB counter Data Register bit 8~15 | 82H | 00H |
| MIB_DAT | MIB counter Data Register bit 16~23 | 83H | 00H |
| MIB_DAT | MIB counter Data Register bit 24~31 | 84H | 00H |
| PVLAN | Port-based VLAN mapping table registers | B0-BFH | 0FH |
| TOS_MAP | TOS Priority Map Register | C0-CFH | 00H~FFH |
| VLAN_MAP | VLAN priority Map Register | D0-D1H | 50H,FAH |
| MEM_CNTRL | Memory Access Control | F0H | |
| MRRL | Memory Address Register Low Byte | F1H | |
| MRRH | Memory Address Register High Byte | F2H | |
| MRCMDX | Memory Read Without Address Increment | F3H | |
| MRCMD | Memory Read With Address Increment | F4H | |
| MW_WORD | Memory Write Word Data | F5H | |
| MW_LOW | Memory Write Low Byte Data | F6H | |
| MW_HIGH | Memory Write High Byte Data | F7H | |

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>, <Access Type>

Where:

<Reset Value>:

- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value

P = power on and hardware reset default value

S = software reset, by Reg. 52H bit 6, default value

E = default value from EEPROM setting

T = default value from strap pin

<Access Type>:

RO = Read only

RW = Read/Write

R/C = Read and Clear

RW/C1=Read/Write and Cleared by write 1

WO = Write only

Reserved bits should be written with 0.

Reserved bits are undefined on read access.

6.1 EEPROM Control Register (0AH)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|--|
| 7 | RESERVED | — | RO | Reserved |
| 6 | EE_TYPE | — | PS0,RW | EEPROM Type Select This bit works after power-on EEPROM loading done. 0: 93C46(Default) 1: 93C56/66 |
| 5:0 | RESERVED | — | RO | Reserved |

6.2 EEPROM & PHY Control Register (0BH)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|--|
| 7 | RESERVED | — | RO | Reserved |
| 6 | EE_TYPE | — | PS0,RO | EEPROM Type Status 0: 93C46(Default) 1: 93C56/66 |
| 5 | REEP | — | PS0,RW | Reload EEPROM. Driver needs to clear it up after the operation completes |
| 4 | WEP | — | PS0,RW | Write EEPROM Enable |
| 3 | EPOS | — | PS0,RW | EEPROM or PHY Operation Select When reset, select EEPROM; when set, select PHY |
| 2 | ERPRR | — | PS0,RW | EEPROM Read or PHY Register Read Command. Driver needs to clear it up after the operation completes. |
| 1 | ERPRW | — | PS0,RW | EEPROM Write or PHY Register Write Command. Driver needs to clear it up after the operation completes. |
| 0 | ERRE | — | PS0,RO | EEPROM Access Status or PHY Access Status When set, it indicates that the EEPROM or PHY access is in progress |

6.3 EEPROM & PHY Address Register (0CH)

| Bit | Name | ROM | Default | Description |
|-----|---------|-----|---------|---|
| 7:6 | PHY_ADR | — | PS0,RW | PHY Address bit 1 and 0; the PHY address bit [4:2] is force to 0. |
| 5:0 | EROA | — | PS0,RW | EEPROM Word Address or PHY Register Address |

6.4 EEPROM & PHY Data Register (0DH~0EH)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|---|
| 7:0 | EE_PHY_L | — | PS0,RW | EEPROM or PHY Low Byte Data (0DH) This data is made to write/read low byte of word address defined in Reg.0CH to EEPROM or PHY |
| 7:0 | EE_PHY_H | — | PS0,RW | EEPROM or PHY High Byte Data (0EH) This data is made to write/read high byte of word address defined in Reg.0CH to EEPROM or PHY |

6.5 Vendor ID Registers (28H~29H)

| Bit | Name | ROM | Default | Description |
|-----|------|---------|-----------|---------------------------|
| 7:0 | VIDH | 4[15:8] | PE,0AH,RO | Vendor ID High Byte (29H) |
| 7:0 | VIDL | 4[7:0] | PE,46H,RO | Vendor ID Low Byte (28H) |

6.6 Product ID Registers (2AH~2BH)

| Bit | Name | ROM | Default | Description |
|-----|------|---------|-----------|----------------------------|
| 7:0 | PIDH | 5[15:8] | PE,82H,RO | Product ID High Byte (2BH) |
| 7:0 | PIDL | 5[7:0] | PE,03H,RO | Product ID Low Byte (2AH) |

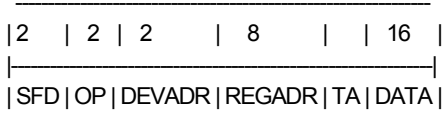


6.7 Chip Revision Register (2CH)

| Bit | Name | ROM | Default | Description |
|-----|-------|-----|----------|---------------|
| 7:0 | CHIPR | — | P,03H,RO | CHIP Revision |

Because SMI bus tends to be interfered by noise on board-level.
 This function is used to check the command validity to suppress the mistaken command.

SMI Format:



- SFD: Start of Frame Delimiter (2'b01)
- OP: Operation Code (Read=2'b10, Write=2'b01)
- DEVADR: Device Address
- REGADR: Address for internal register of PHY device
- DATA : Data field.
 Driven by STA for write, Driven by PHY for read.

Example:

```

1. Write Reg37h with 0x80 // SMI Bus Error Check Enable

//-- Write Command Flow
2. Write RegF1h with 0x82 // Any register you want to write
3. Write Reg36h with 0xXX // CPU Write Command Checksum of step 2 (Error proofing)
4. Read Reg37h // Check Reg37h.[0] (Error detecting)
5. Read Reg36h // Check read Reg37h checksum of step 4(Error proofing)

//-- Read Command Flow
6. Read RegF1h
7. Read Reg36h // Check Reg36h by CPU
// (Error proofing & detecting)
  
```

Checksum Formula:

```

CSUM[0] = DATA[0] ^ DATA[8] ^ REGADR[0] ^ DEVADR[0];
CSUM[1] = DATA[1] ^ DATA[9] ^ REGADR[1] ^ DEVADR[1];
CSUM[2] = DATA[2] ^ DATA[10] ^ REGADR[2] ^ OP[0];
CSUM[3] = DATA[3] ^ DATA[11] ^ REGADR[3] ^ OP[1];
CSUM[4] = DATA[4] ^ DATA[12] ^ REGADR[4];
CSUM[5] = DATA[5] ^ DATA[13] ^ REGADR[5];
CSUM[6] = DATA[6] ^ DATA[14] ^ REGADR[6];
CSUM[7] = DATA[7] ^ DATA[15] ^ REGADR[7];
  
```

6.8 Port 2 driving capability Register (3AH)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|---|
| 7 | RESERVED | — | RO | Reserved |
| 6:5 | P2_CURR | | P01,RW | Port 2 TXD/TXE Current Driving/Sinking Capability 00: 2mA 01: 4mA (default) 10: 6mA 11: 8mA |
| 4:0 | RESERVED | — | RO | Reserved |

6.9 Port 2 MAC Control Register (3BH)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|--|
| 7:4 | RESERVED | — | RO | Reserved |
| 3 | P2_MODE | — | PST0,RW | Port2 status in auto-polling mode for MII/RevMII/RMII 0: auto-polling mode 1: force mode |
| 2 | P2_LINK | — | PS0,RW | When Port2 in force mode for MII/RevMII/RMII 0: link ON 1: link OFF |
| 1 | P2_DPX | — | PS0,RW | When Port2 in force mode for MII/RevMII/RMII 0: Full-duplex mode 1: Half-duplex mode |
| 0 | P2_SPEED | — | PST0,RW | When Port2 in force mode for MII/RevMII/RMII 0: 100M mode 1: 10M mode |

6.10 PHY Control Register (3CH)

| Bit | Name | ROM | Default | Description |
|-----|-----------------|-------|--------------|--|
| 7 | MDIX_DIS_P 0 | 7[15] | PSE0,RW | Port0 Auto-MDIX Control 0: Auto_MDIX Enable 1: Auto_MDIX Disable |
| 6 | MDIX_DIS_P 1 | 7[14] | PSE0,RW | Port1 Auto-MDIX Control 0: Auto_MDIX Enable 1: Auto_MDIX Disable |
| 5:1 | RESERVED | — | RO | Reserved |
| 0 | PHY_LFP_E N | 7[8] | PSET0,R W | PHY LFP Control 0: PHY LFP Disable 1: PHY LFP Enable |

6.11 PHY Control Test Register (3EH)

| Bit | Name | ROM | Default | Description |
|-----|-----------|-----|---------|--|
| 7:4 | RESERVED | — | RO | Reserved |
| 3:0 | I_TUNE_TX | — | PS3,RW | TX Operation Current To tune the TX operation current |

6.12 Monitor Strap pin & enable pin status Register 1 (41H)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|------------------|
| 7 | H_TEST3 | --- | PT,RO | hard-strap TEST3 |
| 6 | H_TEST2 | --- | PT,RO | hard-strap TEST2 |
| 5 | H_TEST1 | --- | PT,RO | hard-strap TEST1 |
| 4 | H_MDC | --- | PTRO | hard-strap MDC |
| 3 | RESERVED | --- | RO | Reserved |
| 2 | H_EECS | --- | PT,RO | hard-strap EECS |
| 1 | H_EECK | --- | PT,RO | hard-strap EECK |
| 0 | RESERVED | --- | RO | Reserved |

6.13 Monitor Strap pin & enable pin status Register 2 (42H)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|------------------------------|
| 7:6 | RESERVED | --- | RO | Reserved |
| 5 | HS_TXER2 | --- | PT,RW | hard-strap/soft-strap TXER2 |
| 4 | HS_TXE2 | --- | PT,RW | hard-strap/soft-strap TXE2 |
| 3 | HS_TXD23 | --- | PT,RW | hard-strap/soft-strap TXD2_3 |
| 2 | HS_TXD22 | --- | PT,RW | hard-strap/soft-strap TXD2_3 |
| 1 | HS_TXD21 | --- | PT,RW | hard-strap/soft-strap TXD2_3 |
| 0 | HS_TXD20 | --- | PT,RW | hard-strap/soft-strap TXD2_3 |

6.14 Switch Control Register 1 (52H)

| Bit | Name | ROM | Default | Description | | | | | | | | |
|-----|----------|---------|---------|---|----|--------|----|--------|----|--------|----|----------|
| 7 | RESERVED | --- | RO | Reserved | | | | | | | | |
| 6 | RST_SW | --- | P0,RW | Reset Switch Core and auto clear after 10us | | | | | | | | |
| 5 | RST_ANLG | --- | P0,RW | Reset Analog PHY Core and auto clear after 10us | | | | | | | | |
| 4:3 | SNF_PORT | 17[4:3] | PSE0,RW | Sniffer Port Number Define the port number to act as the sniffer port <table border="1" style="margin-left: 20px;"> <tr> <td>00</td> <td>Port 0</td> </tr> <tr> <td>01</td> <td>Port 1</td> </tr> <tr> <td>10</td> <td>Port 2</td> </tr> <tr> <td>11</td> <td>Reserved</td> </tr> </table> | 00 | Port 0 | 01 | Port 1 | 10 | Port 2 | 11 | Reserved |
| 00 | Port 0 | | | | | | | | | | | |
| 01 | Port 1 | | | | | | | | | | | |
| 10 | Port 2 | | | | | | | | | | | |
| 11 | Reserved | | | | | | | | | | | |
| 2 | CRC_DIS | 17[2] | PSE0,RW | CRC Checking Disable When set, the received CRC error packet also accepts to receive memory. | | | | | | | | |
| 1:0 | AGE | 17[1:0] | PSE0,RW | Address Table Aging 00: no aging 01: 64 ± 32 sec 10: 128 ± 64 sec 11: 256 ± 128 sec | | | | | | | | |

6.15 VLAN Control Register 1 (53H)

| Bit | Name | ROM | Default | Description |
|-----|----------|--------|---------|---|
| 7 | TOS6 | 17[15] | PSE0,RW | Full IP ToS Field for Priority Queue 1: check most significant 6-bit of TOS 0: check most significant 3-bit only of TOS |
| 6 | RESERVED | — | RO | Reserved |
| 5 | UNICAST | 17[13] | PSE0,RW | Unicast packet can across VLAN boundary |
| 4 | VIDFF | 17[12] | PSE0,RW | Replace VIDFF If the received packet is a tagged VLAN with VID equal to "FFF", its VLAN field is replaced with VLAN tag defined in Reg. 6EH and 6FH. |
| 3 | VID1 | 17[11] | PSE0,RW | Replace VID01 If the received packet is a tagged VLAN with VID equal to "001", its VLAN field is replaced with VLAN tag defined in Reg. 6EH and 6FH. |
| 2 | VID0 | 17[10] | PSE0,RW | Replace VID0 If the received packet is a tagged VLAN with VID equal to "000", its VLAN field is replaced with VLAN tag defined in Reg. 6EH and 6FH. |
| 1 | PRI | 17[9] | PSE0,RW | Replace priority field in the tag with value define in Reg 6FH bit 7~5. |
| 0 | VLAN | 17[8] | PSE0,RW | VLAN mode enable 1: 802.1Q base VLAN mode enable 0: port-base VLAN only |

6.16 Switch Status Register (54H)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|--|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | RESERVED | — | RO | Reserved |
| 1 | EACMEMST | — | PS0,RO | Memory BIST Status (11K) 0: Pass 1: Fail |
| 0 | RXMEMST | — | PS0,RO | Memory BIST Status (24K) 0: Pass 1: Fail |

6.17 Switch Control Register 2 (55H)

| Bit | Name | ROM | Default | Description |
|-----|-----------|-----|---------|---|
| 7 | RESERVED | — | RO | Reserved |
| 6 | FDX_FLOW | — | PS0,RW | Flow Control Option When set In full duplex mode, if link partner's flow control capability is disabled, the flow control of DM8203I corresponding port is also disabled. When this is "0", the flow control is controlled by register 61H bit 4. |
| 5 | LRN_PAUSE | — | PS0,RW | Learn PAUSE Frame 0: Disable (default) 1: Enable |



| | | | | |
|-----|-----------|---|--------|---|
| 4 | LRN_VLAN | — | PS0,RW | Address Learning Consider VLAN Member 0: Address learning despite VLAN member (default) 1: Address learning is disable, if incoming port doesn't exist in its member set. |
| 3 | MIRR_PAIR | — | PS0,RW | Mirror RX/TX Pair Mode Enable 0: Disable (default) 1: Enable |
| 2:0 | RESERVED | — | RO | Reserved |

6.18 VLAN Control Register 2 (56H)

| Bit | Name | ROM | Default | Description |
|-----|------------|-----|---------|--|
| 7 | FIR_VIDFFF | | PS0,RW | Drop Packet with VID==0xFFF Enable 0: Disable 1: Enable |
| 6 | FIR_CFI | | PS0,RW | Drop Packet with Nonzero CFI Enable Drop incoming packet, if the CFI field is not equal to zero. 0: Disable 1: Enable |
| 5:0 | RESERVED | | RO | Reserved |

6.19 Per Port Control/Status Index Register (60H)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|---|
| 7:2 | RESERVED | — | RO | Reserved |
| 1:0 | INDEX | — | PS0,RW | Port index for register 61h~73h Write the port number to this register before write/read register 61h~73h. |

6.20 Per Port Control Data Register (61H)

| Bit | Name | ROM | Default | Description |
|-----|-----------|-------------|---------|---|
| 7 | RESERVED | — | RO | Reserved |
| 6 | PARTI_EN | 19,21,23[6] | PSE0,RW | Enable Partition Detection |
| 5 | NO_DIS_RX | 19,21,23[5] | PSE0,RW | Not Discard RX Packets when Ingress Bandwidth Control When received packets bandwidth reach Ingress bandwidth threshold, the packets over the threshold are not discarded but with flow control. |
| 4 | FLOW_DIS | 19,21,23[4] | PSE0,RW | Flow control in full duplex mode, or back pressure in half duplex mode enable 0 – enable 1 – disable |
| 3 | BANDWIDTH | 19,21,23[3] | PSE0,RW | Bandwidth Control 0: Control with Ingress and Egress separately, ref to Register 66h. 1: Control with Ingress or Egress, ref to Register 67h |
| 2 | BP_DIS | 19,21,23[2] | PSE0,RW | Broadcast packet filter 0 – accept broadcast packets 1 – reject broadcast packets |



| | | | | |
|---|----------|-------------|---------|---|
| 1 | MP_DIS | 19,21,23[1] | PSE0,RW | Multicast packet filter 0 – accept multicast packets 1 – reject multicast packets |
| 0 | MP_STORM | 19,21,23[0] | PSE0,RW | Broadcast Storm Control 0 – only broadcast packets storm are controlled 1 – Multicast packets also same as broadcast storm control. |

6.21 Per Port Status Data Register (62H)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|--|
| 7:6 | RESERVED | — | RO | Reserved |
| 5 | LP_FCS | — | P0,RO | Link Partner Flow Control Enable Status |
| 4:3 | RESERVED | — | RO | Reserved |
| 2 | SPEED2 | — | P0,RO | PHY Speed Status 0: 10Mbps, 1:100Mbps |
| 1 | FDX2 | — | P0,RO | PHY Duplex Status 0: half-duplex, 1:full-duplex |
| 0 | LINK2 | — | P0,RO | PHY Link Status 0: link fail, 1: link OK |

6.22 Per Port Forward Control Register 1 (63H)

| Bit | Name | ROM | Default | Description |
|-----|----------------|-----|---------|--|
| 7 | HOB_DIS | — | PS0,RW | Head-of-Line Blocking Prevent Control 0: Disable (Default) 1: Enable |
| 6 | DIS_PAUSE | — | PS0,RW | Maximum Pause Packet from Link Partner 0: always care pause packet from link partner(default) 1: pause packet by passed after 7 continued pause packet from link partner |
| 5 | STORM_UUP | — | PS0,RW | Storm Enable for Un-learned Unicast DMAC Packets 0: Disable 1: Enable |
| 4 | PAUSE_CO N | — | PS0,RW | Send PAUSE Continuously If buffer congestion occur on full duplex, switch will send PAUSE frames: 0: Up to 8-times(default) 1: Continuously until alleviation |
| 3 | RESERVED | — | RO | Reserved |
| 2 | FIR_UMDMA C | — | PS0,RW | Filter Packets with Un-learned Multicast DMAC 0: Disable 1: Enable |
| 1 | FIR_MSMAC | — | PS0,RW | Filter Packets with Multicast SMAC 0: Disable 1: Enable |
| 0 | FIR_UUDMA C | — | PS0,RW | Filter Packets with Un-learned Unicast DMAC 0: Disable 1: Enable |

6.23 Per Port Forward Control Register 2 (64H)

| Bit | Name | ROM | Default | Description |
|-----|------------|-----|---------|---|
| 7:4 | RESERVED | — | RO | Reserved |
| 3:2 | MAX_PKTLEN | — | PS0,RW | Max Packet Length 00: 1536-bytes 01: 1552-bytes 10: 1800-bytes 11: 2032-bytes |
| 1:0 | RESERVED | — | RO | Reserved |

6.24 Per Port Forward Control Register 3 (65H)

| Bit | Name | ROM | Default | Description |
|-----|---------------|-----|---------|---|
| 7 | LOOPBACK | — | PS0,RW | Loop-Back Mode The transmitted packet will be forward to this port itself. |
| 6 | MONI_TX | — | PS0,RW | TX Packet Monitored The transmitted packets are also forward to sniffer port. |
| 5 | MONI_RX | — | PS0,RW | RX Packet Monitored The received packets are also forward to sniffer port. |
| 4 | DIS_BMP | — | PS0,RW | Broad/Multicast Not Monitored The received broadcast or multicast packets are not forward to sniffer port. |
| 3 | UNPLUG_CLEARS | — | PS0,RW | Unplug Clear Address Enable Enable to automatically clear address record in address table after unplug 0: Disable, retaining address record (Default) 1: Enable, clearing address record |
| 2 | TX_DIS | — | PS0,RW | Packet Transmit Disabled All packets cannot be forward to this port. |
| 1 | RX_DIS | — | PS0,RW | Packet receive Disabled All received packets are discarded. |
| 0 | ADR_DIS | — | PS0,RW | Address Learning Disabled The Source Address (SA) field of packet is not learned to address table. |

6.25 Per Port Ingress/Egress Control Register (66H)

| Bit | Name | ROM | Default | Description |
|-----|---------|-------------------------------------|---------|---|
| 7:4 | INGRESS | 19[15:12] 21[15:12] 23[15:12] | PSE0,RW | <p>Ingress Rate Control</p> <p>These bits define the bandwidth threshold that received packets over the threshold are discarded.</p> <p>0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps</p> |
| 3:0 | EGRESS | 19[11:8] 21[11:8] 23[11:8] | PSE0,RW | <p>Egress Rate Control</p> <p>These bits define the bandwidth threshold that transmitted packets over the threshold are discarded.</p> <p>0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps</p> |

6.26 Bandwidth Control Setting Register (67H)

| Bit | Name | ROM | Default | Description |
|-----|---------|-------------------------------|---------|--|
| 7:4 | BSTH | 20[7:4] 22[7:4] 24[7:4] | PSE0,RW | Broadcast Storm Threshold These bits define the bandwidth threshold that received broadcast packets over the threshold are discarded 0000: no broadcast storm control 0001: 8K packets/sec 0010: 16K packets/sec 0011: 64K packets/sec 0100: 5% 0101: 10% 0110: 20% 0111: 30% 1000: 40% 1001: 50% 1010: 60% 1011: 70% 1100: 80% 1101: 90% 111X: no broadcast storm control |
| 3:0 | BW CTRL | 20[3:0] 22[3:0] 24[3:0] | PSE0,RW | Received and Transmitted Bandwidth Control These bits define the bandwidth threshold that transmitted or received packets over the threshold are discarded 0000: none 0001: 64Kbps 0010: 128Kbps 0011: 256Kbps 0100: 512Kbps 0101: 1Mbps 0110: 2Mbps 0111: 4Mbps 1000: 8Mbps 1001: 16Mbps 1010: 32Mbps 1011: 48Mbps 1100: 64Mbps 1101: 72Mbps 1110: 80Mbps 1111: 88Mbps |

6.27 Per Port Block Unicast ports Control Register (68H)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|--|
| 7:3 | RESERVED | — | RO | Reserved |
| 2:0 | BLK_UP | — | PS0,RW | Ports of Unicast Packet Be Blocked The received unicast packets are not forward to the assigned ports. Note that the assigned port definition: bit 0 for port 0, bit 1 for port 1, |

6.28 Per Port Block Multicast ports Control Register (69H)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|---|
| 7:3 | RESERVED | — | RO | Reserved |
| 2:0 | BLK_MP | — | PS0,RW | Ports of Multicast Packet Be Blocked The received multicast packets are not forward to the assigned ports. |

6.29 Per Port Block Broadcast ports Control Register (6AH)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|---|
| 7:3 | RESERVED | — | RO | Reserved |
| 2:0 | BLK_BP | — | PS0,RW | Ports of Broadcast Packet Be Blocked The received broadcast packets are not forward to the assigned ports. |

6.30 Per Port Block Unknown ports Control Register (6BH)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|---|
| 7:3 | RESERVED | — | RO | Reserved |
| 2:0 | BLK_UKP | — | PS0,RW | Ports of Unknown Packet Be Blocked The packets with DA field not found in address table are not forward to the assigned ports. |

6.31 Per Port Priority & VLAN Control Register (6CH)

| Bit | Name | ROM | Default | Description |
|-----|-------------|-----|---------|---|
| 7:6 | RESERVED | — | RO | Reserved |
| 5 | FIR_VIPOINT | — | PS0,RW | Enable to Filter Packet with Incoming Port is Non-member in VLAN 0: Disable 1: Enable |
| 4 | NOTAG_IN | — | PS0,RW | Input Force No Tag Assume all received frame are untagged 0: Disable 1: Enable |
| 3:2 | RESERVED | — | RO | Reserved |



| | | | | |
|-----|----------|---|--------|---|
| 1:0 | VLAN_IAC | — | PS0,RW | VLAN Ingress Admit Only Control 00: Accept all frames 01: Accept VLAN-tagged frames only Untagged or priority tagged(VID=0) frames will be dropped 10: Accept untagged frames only 11: Accept frame's VID equal to ingress PVID |
|-----|----------|---|--------|---|

6.32 Per Port Priority Queue Control Register (6DH)

| Bit | Name | ROM | Default | Description |
|-----|---------|-------------------------------|---------|--|
| 7 | TAG_OUT | 20[15] 22[15] 24[15] | PSE0,RW | Output Packet Tagging Enable The transmitted packets are containing VLAN tagged field. |
| 6 | PRI_DIS | 20[14] 22[14] 24[14] | PSE0,RW | Priority Queue Disable Only one transmit queue is supported in this port. |
| 5 | WFQUE | 20[13] 22[13] 24[13] | PSE0,RW | Weighted Fair Queuing 1: The priority weight for queue 3, 2, 1, and 0 is 8, 4, 2, and 1 respectively. 0: The queue 3 has the highest priority, and the next priorities are queue 2, 1, and 0 respectively. |
| 4 | TOS_PRI | 20[12] 22[12] 24[12] | PSE0,RW | Priority ToS over VLAN If an IP packet with VLAN tag, the priority of this packet is decode from ToS field. |
| 3 | TOS_OFF | 20[11] 22[11] 24[11] | PSE0,RW | ToS Priority Classification Disable The priority information from ToS field of IP packet is ignored. |
| 2 | PRI_OFF | 20[10] 22[10] 24[10] | PSE0,RW | 802.1 p Priority Classification Disable The priority information from VLAN tag field is ignored. |
| 1:0 | P_PRI | 20[9:8] 22[9:8] 24[9:8] | PSE0,RW | Port Base priority The priority queue number in port base. 00= queue 0, 01=queue 1, 10=queue 2, 11=queue 3 |

6.33 Per Port VLAN Tag Low Byte Register (6EH)

| Bit | Name | ROM | Default | Description |
|-----|-------|-------------------------------|--------------|-------------|
| 7:0 | VID70 | 27[7:0] 28[7:0] 29[7:0] | PSE01,R W | VID[7:0] |

6.34 Per Port VLAN Tag High Byte Register (6FH)

| Bit | Name | ROM | Default | Description |
|-----|------|-------------------------------------|---------|-------------|
| 7:5 | PRI | 27[15:13] 28[15:13] 29[15:13] | PSE0,RW | Tag [15:13] |
| 4 | CFI | 27[12] 28[12] 29[12] | PSE0,RW | Tag[12] |



| | | | | |
|-----|--------|----------------------------------|---------|-----------|
| 3:0 | VID118 | 27[11:8] 28[11:8] 29[11:8] | PSE0,RW | VID[11:8] |
|-----|--------|----------------------------------|---------|-----------|

6.35 MIB counters Port Index Register (80H)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|--|
| 7 | READY | — | PS,RO | MIB counter data is ready When this register is written with INDEX data, this bit is cleared and the MIB counter reading is in progress. After end of read MIB counter, the MIB data is loaded into register 81H~84H, and this bit is set to indicate that the MIB data is ready. |
| 6 | MIB_DIS | — | PS,RW | MIB Counter Disable 0: MIB counter is enabled 1: MIB counter is disabled |
| 5 | RESERVED | — | RO | Reserved |
| 4:0 | INDEX | — | PS,RO | MIB counter index 0~9, each counter is 32-bit in Register 81h~84h. Write the MIB counter index to this register before read them. |

6.36 MIB counter Data Register (81H~84H)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|--------------------------|
| 81H | Counter0 | — | PS,RO | Counter's data bit 7~0 |
| 82H | Counter1 | — | PS,RO | Counter's data bit 15~8 |
| 83H | Counter2 | — | PS,RO | Counter's data bit 23~16 |
| 84H | Counter3 | — | PS,RO | Counter's data bit 31~24 |

MIB counter: RX Byte Counter Registers (INDEX 00H)

MIB counter: RX Uni-cast Packet Counter Registers (INDEX 01H)

MIB counter: RX Multi-cast Packet Counter Registers (INDEX 02H)

MIB counter: RX Discard Packet Counter Registers (INDEX 03H)

MIB counter: RX Error Packet Counter Registers (INDEX 04H)

MIB counter: TX Byte Counter Registers (INDEX 05H)

MIB counter: TX Uni-cast Packet Counter Registers (INDEX 06H)

MIB counter: TX Multi-cast Packet Counter Registers (INDEX 07H)

MIB counter: TX Discard Packet Counter Registers (INDEX 08H)

MIB counter: TX Error Packet Counter Registers (INDEX 09H)

6.37 VLAN grouping table Registers (B0H~BFH)

Define the port member in VLAN group

There are 16 VLAN group that defined in Reg. B0H~BFH.

Group 0 defined in Reg. B0H, and group 1 defined in Reg. B1H ... and so on.

B0H: VLAN 0 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|-------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 32[2] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 32[1] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 32[0] | PSE1,RW | Mapping to port 0 |

B1H: VLAN 1 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|--------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 32[10] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 32[9] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 32[8] | PSE1,RW | Mapping to port 0 |

B2H: VLAN 2 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|-------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 33[2] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 33[1] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 33[0] | PSE1,RW | Mapping to port 0 |

B3H: VLAN 3 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|--------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 33[10] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 33[9] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 33[8] | PSE1,RW | Mapping to port 0 |

B4H: VLAN 4 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|-------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 34[2] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 34[1] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 34[0] | PSE1,RW | Mapping to port 0 |



B5H: VLAN 5 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|--------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 34[10] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 34[9] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 34[8] | PSE1,RW | Mapping to port 0 |

B6H: VLAN 6 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|-------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 35[2] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 35[1] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 35[0] | PSE1,RW | Mapping to port 0 |

B7H: VLAN 7 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|--------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 35[10] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 35[9] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 35[8] | PSE1,RW | Mapping to port 0 |

B8H: VLAN 8 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|-------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 36[2] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 36[1] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 36[0] | PSE1,RW | Mapping to port 0 |

B9H: VLAN 9 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|--------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 36[10] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 36[9] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 36[8] | PSE1,RW | Mapping to port 0 |

BAH: VLAN 10 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|-------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 37[2] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 37[1] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 37[0] | PSE1,RW | Mapping to port 0 |

**BBH: VLAN 11 Grouping**

| Bit | Name | ROM | Default | Description |
|-----|----------|--------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 37[10] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 37[9] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 37[8] | PSE1,RW | Mapping to port 0 |

BCH: VLAN 12 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|-------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 38[2] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 38[1] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 38[0] | PSE1,RW | Mapping to port 0 |

BDH: VLAN 13 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|--------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 38[10] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 38[9] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 38[8] | PSE1,RW | Mapping to port 0 |

BEH: VLAN 14 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|-------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 39[2] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 39[1] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 39[0] | PSE1,RW | Mapping to port 0 |

BFH: VLAN 15 Grouping

| Bit | Name | ROM | Default | Description |
|-----|----------|--------|---------|-------------------|
| 7:4 | RESERVED | — | RO | Reserved |
| 2 | PORT_P2 | 39[10] | PSE1,RW | Mapping to port 2 |
| 1 | PORT_P1 | 39[9] | PSE1,RW | Mapping to port 1 |
| 0 | PORT_P0 | 39[8] | PSE1,RW | Mapping to port 0 |

6.38 TOS Priority Map Registers (C0H~CFH)

Define the 6-bit or 3-bit of ToS field mapping to 2-bit priority queue number.

In 6-bit type, the Reg. 53H bit 7 is "1", Reg. C0H bit [1:0] define the mapping for ToS value 0, Reg. 60H bit [3:2] define the mapping for ToS value 1, ... and so on, till Reg. CFH bit [7:6] define ToS value 63.

In 3-bit type, Reg. C0H bit [1:0] defines the mapping for ToS value 0, Reg. 60H bit [3:2] defines the mapping for ToS value 1 ... and so on, and till Reg. C1H bit [7:6] define ToS value 7.

C0H:

| Bit | Name | ROM | Default | Description |
|-----|------|---------|---------|---|
| 7:6 | TOS3 | 40[7:6] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=03H, otherwise TOS[7:5]=03H |
| 5:4 | TOS2 | 40[5:4] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=02H, otherwise TOS[7:5]=02H |
| 3:2 | TOS1 | 40[3:2] | PSE0,RW | If bit 53H.7 =1 :TOS[7:2]=01H, otherwise TOS[7:5]=01H |
| 1:0 | TOS0 | 40[1:0] | PSE0,RW | If bit 53H.7 =1 :TOS[7:2]=00H, otherwise TOS[7:5]=00H |

C1H:

| Bit | Name | ROM | Default | Description |
|-----|------|-----------|---------|---|
| 7:6 | TOS7 | 40[15:14] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=07H, otherwise TOS[7:5]=07H |
| 5:4 | TOS6 | 40[13:12] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=06H, otherwise TOS[7:5]=06H |
| 3:2 | TOS5 | 40[11:10] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=05H, otherwise TOS[7:5]=05H |
| 1:0 | TOS4 | 40[9:8] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=04H, otherwise TOS[7:5]=04H |

C2H:

| Bit | Name | ROM | Default | Description |
|-----|------|---------|---------|-------------------------------|
| 7:6 | TOSB | 41[7:6] | PSE0,RW | If bit 53H.7 =1 :TOS[7:2]=0BH |
| 5:4 | TOSA | 41[5:4] | PSE0,RW | If bit 53H.7 =1 :TOS[7:2]=0AH |
| 3:2 | TOS9 | 41[3:2] | PSE0,RW | If bit 53H.7 =1 :TOS[7:2]=09H |
| 1:0 | TOS8 | 41[1:0] | PSE0,RW | If bit 53H.7 =1 :TOS[7:2]=08H |

C3H:

| Bit | Name | ROM | Default | Description |
|-----|------|-----------|---------|-------------------------------|
| 7:6 | TOSF | 41[15:14] | PSE0,RW | If bit 53H.7 =1 :TOS[7:2]=0FH |
| 5:4 | TOSE | 41[13:12] | PSE0,RW | If bit 53H.7 =1 :TOS[7:2]=0EH |
| 3:2 | TOSD | 41[11:10] | PSE0,RW | If bit 53H.7 =1 :TOS[7:2]=0DH |
| 1:0 | TOSC | 41[9:8] | PSE0,RW | If bit 53H.7 =1 :TOS[7:2]=0CH |

C4H:

| Bit | Name | ROM | Default | Description |
|-----|-------|---------|---------|-------------------------------|
| 7:6 | TOS13 | 42[7:6] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=13H |
| 5:4 | TOS12 | 42[5:4] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=12H |
| 3:2 | TOS11 | 42[3:2] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=11H |
| 1:0 | TOS10 | 42[1:0] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=10H |



C5H:

| Bit | Name | ROM | Default | Description |
|-----|-------|-----------|---------|-------------------------------|
| 7:6 | TOS17 | 42[15:14] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=17H |
| 5:4 | TOS16 | 42[13:12] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=16H |
| 3:2 | TOS15 | 42[11:10] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=15H |
| 1:0 | TOS14 | 42[9:8] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=14H |

C6H:

| Bit | Name | ROM | Default | Description |
|-----|-------|---------|---------|-------------------------------|
| 7:6 | TOS1B | 43[7:6] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=1BH |
| 5:4 | TOS1A | 43[5:4] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=1AH |
| 3:2 | TOS19 | 43[3:2] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=19H |
| 1:0 | TOS18 | 43[1:0] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=18H |

C7H:

| Bit | Name | ROM | Default | Description |
|-----|-------|-----------|---------|-------------------------------|
| 7:6 | TOS1F | 43[15:14] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=1FH |
| 5:4 | TOS1E | 43[13:12] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=1EH |
| 3:2 | TOS1D | 43[11:10] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=1DH |
| 1:0 | TOS1C | 43[9:8] | PSE1,RW | If bit 53H.7 =1 :TOS[7:2]=1CH |

C8H:

| Bit | Name | ROM | Default | Description |
|-----|-------|---------|---------|-------------------------------|
| 7:6 | TOS23 | 44[7:6] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=23H |
| 5:4 | TOS22 | 44[5:4] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=22H |
| 3:2 | TOS21 | 44[3:2] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=21H |
| 1:0 | TOS20 | 44[1:0] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=20H |

C9H:

| Bit | Name | ROM | Default | Description |
|-----|-------|-----------|---------|-------------------------------|
| 7:6 | TOS27 | 44[15:14] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=27H |
| 5:4 | TOS26 | 44[13:12] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=26H |
| 3:2 | TOS25 | 44[11:10] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=25H |
| 1:0 | TOS24 | 44[9:8] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=24H |

CAH:

| Bit | Name | ROM | Default | Description |
|-----|-------|---------|---------|-------------------------------|
| 7:6 | TOS2B | 45[7:6] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=2BH |
| 5:4 | TOS2A | 45[5:4] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=2AH |
| 3:2 | TOS29 | 45[3:2] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=29H |
| 1:0 | TOS28 | 45[1:0] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=28H |



CBH:

| Bit | Name | ROM | Default | Description |
|-----|-------|-----------|---------|-------------------------------|
| 7:6 | TOS2F | 45[15:14] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=2FH |
| 5:4 | TOS2E | 45[13:12] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=2EH |
| 3:2 | TOS2D | 45[11:10] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=2DH |
| 1:0 | TOS2C | 45[9:8] | PSE2,RW | If bit 53H.7 =1 :TOS[7:2]=2CH |

CCH:

| Bit | Name | ROM | Default | Description |
|-----|-------|---------|---------|-------------------------------|
| 7:6 | TOS33 | 46[7:6] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=33H |
| 5:4 | TOS32 | 46[5:4] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=32H |
| 3:2 | TOS31 | 46[3:2] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=31H |
| 1:0 | TOS30 | 46[1:0] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=30H |

CDH:

| Bit | Name | ROM | Default | Description |
|-----|-------|-----------|---------|-------------------------------|
| 7:6 | TOS37 | 46[15:14] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=37H |
| 5:4 | TOS36 | 46[13:12] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=36H |
| 3:2 | TOS35 | 46[11:10] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=35H |
| 1:0 | TOS34 | 46[9:8] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=34H |

CEH:

| Bit | Name | ROM | Default | Description |
|-----|-------|---------|---------|-------------------------------|
| 7:6 | TOS3B | 47[7:6] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=3BH |
| 5:4 | TOS3A | 47[5:4] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=3AH |
| 3:2 | TOS39 | 47[3:2] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=39H |
| 1:0 | TOS38 | 47[1:0] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=38H |

CFH:

| Bit | Name | ROM | Default | Description |
|-----|-------|-----------|---------|-------------------------------|
| 7:6 | TOS3F | 47[15:14] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=3FH |
| 5:4 | TOS3E | 47[13:12] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=3EH |
| 3:2 | TOS3D | 47[11:10] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=3DH |
| 1:0 | TOS3C | 47[9:8] | PSE3,RW | If bit 53H.7 =1 :TOS[7:2]=3CH |

6.39 VLAN Priority Map Registers (D0H~D1H)

Define the 3-bit of priority field VALN mapping to 2-bit priority queue number.

D0H:

| Bit | Name | ROM | Default | Description |
|-----|------|---------|---------|-------------------------------|
| 7:6 | TAG3 | 31[7:6] | PSE1,RW | VLAN priority tag value = 03H |
| 5:4 | TAG2 | 31[5:4] | PSE1,RW | VLAN priority tag value = 02H |
| 3:2 | TAG1 | 31[3:2] | PSE0,RW | VLAN priority tag value = 01H |
| 1:0 | TAG0 | 31[1:0] | PSE0,RW | VLAN priority tag value = 00H |

D1H:

| Bit | Name | ROM | Default | Description |
|-----|------|-----------|---------|-------------------------------|
| 7:6 | TAG7 | 31[15:14] | PSE3,RW | VLAN priority tag value = 07H |
| 5:4 | TAG6 | 31[13:12] | PSE3,RW | VLAN priority tag value = 06H |
| 3:2 | TAG5 | 31[11:10] | PSE2,RW | VLAN priority tag value = 05H |
| 1:0 | TAG4 | 31[9:8] | PSE2,RW | VLAN priority tag value = 04H |

6.40 Memory Access Enable Register (F0H)

| Bit | Name | ROM | Default | Description |
|-----|----------|-----|---------|---|
| 7 | SEL_RAM | --- | PS0,RW | Memory Access Select 0: for RX 24K SRAM 1: for EAC 11K SRAM |
| 6 | RESERVED | --- | RO | |
| 5 | WRMEM | --- | PS0,RW | Write Memory Enable |
| 4:0 | RESERVED | --- | RO | |

6.41 Memory Low Address Register (F1H)

| Bit | Name | ROM | Default | Description |
|-----|-------|-----|---------|-------------------------|
| 7:0 | MDA_L | --- | PS0,RW | Memory Data Address Low |

6.42 Memory High Address Register (F2H)

| Bit | Name | ROM | Default | Description |
|-----|-------|-----|---------|--------------------------|
| 7:0 | MDA_H | --- | PS0,RW | Memory Data Address High |

6.43 Memory Dummy Read Data Register (F3H)

| Bit | Name | ROM | Default | Description |
|------|------|-----|---------|------------------------|
| 15:0 | MDRD | --- | PS0,RO | Memory Dummy Read Data |

6.44 Memory Read Data Register (F4H)

| Bit | Name | ROM | Default | Description |
|------|------|-----|---------|------------------|
| 15:0 | MRD | --- | PS0,RO | Memory Data Read |

6.45 Memory Write Data Register (F5H)

| Bit | Name | ROM | Default | Description |
|------|------|-----|---------|-------------------|
| 15:0 | MWD | --- | PS0,WO | Memory Write Data |

6.46 Memory Write Bits7~0 Data Register (F6H)

| Bit | Name | ROM | Default | Description |
|------|------|-----|---------|--------------------------------------|
| 15:0 | MWDL | --- | PS0,WO | Memory Write Data Low Bits 7~0 Valid |

6.47 Memory Write Bits15~8 Data Register (F7H)

| Bit | Name | ROM | Default | Description |
|------|------|-----|---------|--|
| 15:0 | MWDH | --- | PS0,WO | Memory Write Data High Bits 15~8 Valid |

7. EEPROM Format

| name | Word | Description |
|------------------|------|--|
| Signature | 0 | When the value is 1049H, this word can be used to check EEPROM type automatically. |
| | 1~2 | Reserved |
| Load Control 0 | 3 | Bit[1:0] = 01: Accept setting of Vendor ID and Product ID Bit[3:2] is reserved, set to "00" or "11" in application. Bit [5:4] is reserved, set to "00" or "11" in application Bit [7:6] is reserved, set to "00" or "11" in application Bit [9:8] is reserved, set to "00" or "11" in application Bit [11:10] is reserved, set to "00" or "11" in application. Bit [13:12] is reserved, set to "00" or "11" in application. Bit[15:14] =01: Accept setting of PHY control |
| Vendor ID | 4 | 2 byte vendor ID (Default: 0A46H), if word 3 bit [1:0] is "01", bit [7:0] will be loaded to Reg.28H bit [15:8] will be loaded to Reg.29H |
| Product ID | 5 | 2 byte product ID (Default: 8203H), if word 3 bit [1:0] is "01", bit [7:0] will be loaded to Reg.2AH bit [15:8] will be loaded to Reg.2BH |
| | 6 | Reserved |
| PHY control | 7 | PHY Auto-MDIX Control if word 3 bit [15:14] is "01", Bit [7:0] Reserved Bit 8: PHY LFP control 1: ON, 0: OFF Bit [13:9] Reserved Bit 14: Port 1 AUTO-MDIX control 1: ON, 0: OFF(default ON) Bit 15: Port 0 AUTO-MDIX control 1: ON 0: OFF(default ON) |
| | 8~15 | Reserved |
| Load Control 1 | 16 | Bit 1:0=01: Accept setting of WORD 17,18 Bit 3:2=01: Accept setting of WORD 19~24 Bit 5:4=01: Accept setting of WORD 27~29 Bit 7:6=01: Accept setting of WORD 31 Bit 9:8=01: Accept setting of WORD 32~39 Bit 11:10=01: Accept setting of WORD 40~47 Bit 15:12 =01: Reserved |
| Switch Control 0 | 17 | When word 16 bit 1:0 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. 52H bit 7~0 This word bit 15~8 will be loaded to Reg. 53H bit 7~0 |
| Switch Control 1 | 18 | When word 16 bit 1:0 is "01", after power on reset: This word bit 7~0 will be loaded to port 0 Reg. 58H bit 7~0 This word bit 15~8 will be loaded to port 0 Reg. 59H bit 7~0 |
| Port 0 Control 0 | 19 | When word 16 bit 3:2 is "01", after power on reset: This word bit 7~0 will be loaded to port 0 Reg. 61H bit 7~0 This word bit 15~8 will be loaded to port 0 Reg. 66H bit 7~0 |
| Port 0 Control 1 | 20 | When word 16 bit 3:2 is "01", after power on reset: This word bit 7~0 will be loaded to port 0 Reg. 67H bit 7~0 |



| | | |
|-----------------------|-------|--|
| | | This word bit 15~8 will be loaded to port 0 Reg. 6DH bit 7~0 |
| Port 1 Control 0 | 21 | When word 16 bit 3:2 is "01", after power on reset: This word bit 7~0 will be loaded to port 1 Reg. 61H bit 7~0 This word bit 15~8 will be loaded to port 1 Reg. 66H bit 7~0 |
| Port 1 Control 1 | 22 | When word 16 bit 3:2 is "01", after power on reset: This word bit 7~0 will be loaded to port 1 Reg. 67H bit 7~0 This word bit 15~8 will be loaded to port 1 Reg. 6DH bit 7~0 |
| Port 2 Control 0 | 23 | When word 16 bit 3:2 is "01", after power on reset: This word bit 7~0 will be loaded to port 2 Reg. 61H bit 7~0 This word bit 15~8 will be loaded to port 2 Reg. 66H bit 7~0 |
| Port 2 Control 1 | 24 | When word 16 bit 3:2 is "01", after power on reset: This word bit 7~0 will be loaded to port 2 Reg. 67H bit 7~0 This word bit 15~8 will be loaded to port 2 Reg. 6DH bit 7~0 |
| | 25-26 | Reserved |
| Port 0 VLAN Tag | 27 | When word 16 bit 5:4 is "01", after power on reset: This word bit 7~0 will be loaded to port 0 Reg. 6EH bit 7~0 This word bit 15~8 will be loaded to port 0 Reg. 6FH bit 7~0 |
| Port 1 VLAN Tag | 28 | When word 16 bit 5:4 is "01", after power on reset: This word bit 7~0 will be loaded to port 1 Reg. 6EH bit 7~0 This word bit 15~8 will be loaded to port 1 Reg. 6FH bit 7~0 |
| Port 2 VLAN Tag | 29 | When word 16 bit 5:4 is "01", after power on reset: This word bit 7~0 will be loaded to port 2 Reg. 6EH bit 7~0 This word bit 15~8 will be loaded to port 2 Reg. 6FH bit 7~0 |
| | 30 | Reserved |
| VLAN Priority Map | 31 | When word 16 bit 7:6 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. D0H bit 7~0 This word bit 15~8 will be loaded to Reg. D1H bit 7~0 |
| Port VLAN Group 0,1 | 32 | When word 16 bit 9:8 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. B0H bit 7~0 This word bit 15~8 will be loaded to Reg. B1H bit 7~0 |
| Port VLAN Group 2,3 | 33 | When word 16 bit 9:8 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. B2H bit 7~0 This word bit 15~8 will be loaded to Reg. B3H bit 7~0 |
| Port VLAN Group 4,5 | 34 | When word 16 bit 9:8 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. B4H bit 7~0 This word bit 15~8 will be loaded to Reg. B5H bit 7~0 |
| Port VLAN Group 6,7 | 35 | When word 16 bit 9:8 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. B6H bit 7~0 This word bit 15~8 will be loaded to Reg. B7H bit 7~0 |
| Port VLAN Group 8,9 | 36 | When word 16 bit 9:8 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. B8H bit 7~0 This word bit 15~8 will be loaded to Reg. B9H bit 7~0 |
| Port VLAN Group 10,11 | 37 | When word 16 bit 9:8 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. B10H bit 7~0 This word bit 15~8 will be loaded to Reg. B11H bit 7~0 |
| Port VLAN Group 12,13 | 38 | When word 16 bit 9:8 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. B12H bit 7~0 This word bit 15~8 will be loaded to Reg. B13H bit 7~0 |
| Port VLAN Group 14,15 | 39 | When word 16 bit 9:8 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. B14H bit 7~0 |



| | | |
|--------------------|----|--|
| | | This word bit 15~8 will be loaded to Reg. B15H bit 7~0 |
| ToS Priority Map 0 | 40 | When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. C0H bit 7~0 This word bit 15~8 will be loaded to Reg. C1H bit 7~0 |
| ToS Priority Map 1 | 41 | When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. C2H bit 7~0 This word bit 15~8 will be loaded to Reg. C3H bit 7~0 |
| ToS Priority Map 2 | 42 | When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. C4H bit 7~0 This word bit 15~8 will be loaded to Reg. C5H bit 7~0 |
| ToS Priority Map 3 | 43 | When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. C6H bit 7~0 This word bit 15~8 will be loaded to Reg. C7H bit 7~0 |
| ToS Priority Map 4 | 44 | When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. C8H bit 7~0 This word bit 15~8 will be loaded to Reg. C9H bit 7~0 |
| ToS Priority Map 5 | 45 | When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. CAH bit 7~0 This word bit 15~8 will be loaded to Reg. CBH bit 7~0 |
| ToS Priority Map 6 | 46 | When word 16 bit 11:10 is "01", after power on reset: This word bit 7~0 will be loaded to Reg. CCH bit 7~0 This word bit 15~8 will be loaded to Reg. CDH bit 7~0 |



8. PHY Registers

MII Register Description

| ADD | Name | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-----|---------------------|------------------------|-------------|--------------|---------------|-------------|------------|-----------------|----------------|--------------------|---------------|------------------|--------------------------------------|---------------|--------------|---------------|------------------|--|
| 00H | CONTR OL | Reset | Loop back | Speed select | Auto-N Enable | Power Down | Isolate | Restart Auto-N | Full Duplex | Coll. Test | Reserved | | | | | | | |
| | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 000_0000 | | | | | | | |
| 01H | STATUS | T4 Cap. | TX FDX Cap. | TX HDX Cap. | 10 FDX Cap. | 10 HDX Cap. | Reserved | | | | Pream. Supr. | Auto-N Compl. | Remote Fault | Auto-N Cap. | Link Status | Jabber Detect | Extd Cap. | |
| | | 0 | 1 | 1 | 1 | 1 | 0000 | | | | 1 | 0 | 0 | 1 | 0 | 0 | 1 | |
| 02H | PHYID1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| 03H | PHYID2 | 1 | 0 | 1 | 1 | 1 | 0 | Model No. 01011 | | | | Version No. 0000 | | | | | | |
| 04H | Auto-Neg. Advertise | Next Page | FLP Rcv Ack | Remote Fault | Reserved | | FC Adv | T4 Adv | TX FDX Adv | TX HDX Adv | 10 FDX Adv | 10 HDX Adv | Advertised Protocol Selector Field | | | | | |
| 05H | Link Part. Ability | LP Next Page | LP Ack | LP RF | Reserved | | LP FC | LP T4 | LP TX FDX | LP TX HDX | LP 10 FDX | LP 10 HDX | Link Partner Protocol Selector Field | | | | | |
| 06H | Auto-Neg. Expansion | Reserved | | | | | | | | | | Pardet Fault | LP Next Pg Able | Next Pg Able | New Pg Rcv | LP AutoN Cap. | | |
| 10H | Specified Config. | BP 4B5B | BP SCR | BP ALIGN | BP_AD_P OK | Reserve dr | TX | Reserve d | Reserve d | Force 100LNK | Reserve d | Reserve d | RPDCTR -EN | Reset St. Mch | Pream. Supr. | Sleep mode | Reserved | |
| 11H | Specified Conf/Stat | 100 FDX | 100 HDX | 10 FDX | 10 HDX | Reserve d | Reverse d | Reverse d | PHY ADDR [4:0] | | | | Auto-N. Monitor Bit [3:0] | | | | | |
| 12H | 10T Conf/Stat | Rsvd | LP Enable | HBE Enable | SQUE Enable | JAB Enable | Reserve d | Reserved | | | | | | | | | Polarity Reverse | |
| 13H | PWDOR | Reserved | | | | | | | PD10DR V | PD100I | PDchip | PDcm | PDaeq | PDdrv | PDeci | PDeco | PD10 | |
| 14H | Specified config | TSTSE1 | TSTSE2 | Reversed | FORCE_FEF | PREA_MBLE X | TX10M_PWR | NWAY_PWR | Reserved | MDIX_C NTL | AutoNeg_dlpbk | Mdix_fix Value | Mdix_do wn | MonSel1 | MonSel0 | Reserve d | PD_valu e | |
| 16H | RCVER | Receiver Error Counter | | | | | | | | | | | | | | | | |
| 17H | DIS_conn ect | Reversed | | | | | | | | Disconnect_counter | | | | | | | | |
| 1DH | PSCR | Reversed | | | | PREA_MBLE X | AMPLIT_UDE | TX_PW R | Reversed | | | | | | | | | |

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>, <Access Type> / <Attribute(s)>

Where:

<Reset Value>:

- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value

<Access Type>:

RO = Read only, RW = Read/Write

<Attribute (s)>:

SC = Self clearing, P = Value permanently set

8.1 Basic Mode Control Register (BMCR) – 00H

| Bit | Bit Name | Default | Description |
|-----|--------------------------|----------|--|
| 15 | Reset | 0, RW/SC | Reset 1=Software reset 0=Normal operation This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed |
| 14 | Loopback | 0, RW | Loopback Loop-back control register 1 = Loop-back enabled 0 = Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appears at the MII receive outputs |
| 13 | Speed selection | 1, RW | Speed Select 1 = 100Mbps 0 = 10Mbps Link speed may be selected either by this bit or by auto-negotiation. When auto-negotiation is enabled and bit 12 is set, this bit will return auto-negotiation selected medium type |
| 12 | Auto-negotiation enable | 1, RW | Auto-negotiation Enable 1 = Auto-negotiation is enabled, bit 8 and 13 will be in auto-negotiation status |
| 11 | Power down | 0, RW | Power Down While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MII 1=Power down 0=Normal operation |
| 10 | Isolate | 0,RW | Isolate Force to 0 in application. |
| 9 | Restart Auto-negotiation | 0,RW/SC | Restart Auto-negotiation 1 = Restart auto-negotiation. Re-initiates the auto-negotiation process. When auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning to a value of 1 until auto-negotiation is initiated by the DM8203I. The operation of the auto-negotiation process will not be affected by the management entity that clears this bit 0 = Normal operation |
| 8 | Duplex mode | 1,RW | Duplex Mode 1 = Full duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With auto-negotiation enabled, this bit reflects the duplex capability selected by auto-negotiation 0 = Normal operation |



| | | | |
|-----|----------------|------|--|
| 7 | Collision test | 0,RW | Collision Test 1 = Collision test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN in internal MII interface. 0 = Normal operation |
| 6-0 | Reserved | 0,RO | Reserved Read as 0, ignore on write |

8.2 Basic Mode Status Register (BMSR) – 01H

| Bit | Bit Name | Default | Description |
|------|---------------------------|---------|---|
| 15 | 100BASE-T4 | 0,RO/P | 100BASE-T4 Capable 1 = DM8203I is able to perform in 100BASE-T4 mode 0 = DM8203I is not able to perform in 100BASE-T4 mode |
| 14 | 100BASE-TX full-duplex | 1,RO/P | 100BASE-TX Full Duplex Capable 1 = DM8203I is able to perform 100BASE-TX in full duplex mode 0 = DM8203I is not able to perform 100BASE-TX in full duplex mode |
| 13 | 100BASE-TX half-duplex | 1,RO/P | 100BASE-TX Half Duplex Capable 1 = DM8203I is able to perform 100BASE-TX in half duplex mode 0 = DM8203I is not able to perform 100BASE-TX in half duplex mode |
| 12 | 10BASE-T full-duplex | 1,RO/P | 10BASE-T Full Duplex Capable 1 = DM8203I is able to perform 10BASE-T in full duplex mode 0 = DM8203I is not able to perform 10BASE-TX in full duplex mode |
| 11 | 10BASE-T half-duplex | 1,RO/P | 10BASE-T Half Duplex Capable 1 = DM8203I is able to perform 10BASE-T in half duplex mode 0 = DM8203I is not able to perform 10BASE-T in half duplex mode |
| 10-7 | Reserved | 0,RO | Reserved Read as 0, ignore on write |
| 6 | MF preamble suppression | 1,RO | MII Frame Preamble Suppression 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed |
| 5 | Auto-negotiation Complete | 0,RO | Auto-negotiation Complete 1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed |
| 4 | Remote fault | 0, RO | Remote Fault 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM8203I implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0 = No remote fault condition detected |
| 3 | Auto-negotiation ability | 1,RO/P | Auto Configuration Ability 1 = DM8203I is able to perform auto-negotiation 0 = DM8203I is not able to perform auto-negotiation |
| 2 | Link status | 0,RO | Link Status 1 = Valid link is established (for either 10Mbps or 100Mbps operation) |



| | | | |
|---|---------------------|--------|--|
| | | | 0 = Link is not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface |
| 1 | Jabber detect | 0, RO | Jabber Detect 1 = Jabber condition detected 0 = No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a DM8203I reset. This bit works only in 10Mbps mode |
| 0 | Extended capability | 1,RO/P | Extended Capability 1 = Extended register capable 0 = Basic register capable only |

8.3 PHY ID Identifier Register #1 (PHYID1) – 02H

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM8203I. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

| Bit | Bit Name | Default | Description |
|------|----------|---------|---|
| 15-0 | OUI_MSB | <0181h> | OUI Most Significant Bits This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2) |

8.4 PHY ID Identifier Register #2 (PHYID2) – 03H

| Bit | Bit Name | Default | Description |
|-------|----------|----------------|---|
| 15-10 | OUI_LSB | <101110>, RO/P | OUI Least Significant Bits Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively |
| 9-4 | VNDR_MDL | <001011>, RO/P | Vendor Model Number Five bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9) |
| 3-0 | MDL_REV | <0000>, RO/P | Model Revision Number Five bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 4) |

8.5 Auto-negotiation Advertisement Register (ANAR) – 04H

This register contains the advertised abilities of this DM8203I device as they will be transmitted to its link partner during Auto-negotiation.

| Bit | Bit Name | Default | Description |
|-------|----------|-------------|--|
| 15 | NP | 0,RO/P | Next page Indication 0 = No next page available 1 = Next page available The DM8203I has no next page, so this bit is permanently set to 0 |
| 14 | ACK | 0,RO | Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM8203I's auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the auto-negotiation process. Software should not attempt to write to this bit. |
| 13 | RF | 0, RW | Remote Fault 1 = Local device senses a fault condition 0 = No fault detected |
| 12-11 | Reserved | X, RW | Reserved Write as 0, ignore on read |
| 10 | FCS | 0, RW | Flow Control Support 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability |
| 9 | T4 | 0, RO/P | 100BASE-T4 Support 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported The DM8203I does not support 100BASE-T4 so this bit is permanently set to 0 |
| 8 | TX_FDX | 1, RW | 100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the local device 0 = 100BASE-TX full duplex is not supported |
| 7 | TX_HDX | 1, RW | 100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the local device 0 = 100BASE-TX half duplex is not supported |
| 6 | 10_FDX | 1, RW | 10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the local device 0 = 10BASE-T full duplex is not supported |
| 5 | 10_HDX | 1, RW | 10BASE-T Support 1 = 10BASE-T half duplex is supported by the local device 0 = 10BASE-T half duplex is not supported |
| 4-0 | Selector | <00001>, RW | Protocol Selection Bits These bits contain the binary encoded protocol selector supported by this node <00001> indicates that this device supports IEEE 802.3 CSMA/CD |

8.6 Auto-negotiation Link Partner Ability Register (ANLPAR) – 05H

This register contains the advertised abilities of the link partner when received during Auto-negotiation.

| Bit | Bit Name | Default | Description |
|-------|----------|-------------|--|
| 15 | NP | 0, RO | Next Page Indication 0 = Link partner, no next page available 1 = Link partner, next page available |
| 14 | ACK | 0, RO | Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM8203I's auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit |
| 13 | RF | 0, RO | Remote Fault 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner |
| 12-11 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 10 | FCS | 0, RO | Flow Control Support 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner |
| 9 | T4 | 0, RO | 100BASE-T4 Support 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner |
| 8 | TX_FDX | 0, RO | 100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the link partner 0 = 100BASE-TX full duplex is not supported by the link partner |
| 7 | TX_HDX | 0, RO | 100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the link partner 0 = 100BASE-TX half duplex is not supported by the link partner |
| 6 | 10_FDX | 0, RO | 10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the link partner 0 = 10BASE-T full duplex is not supported by the link partner |
| 5 | 10_HDX | 0, RO | 10BASE-T Support 1 = 10BASE-T half duplex is supported by the link partner 0 = 10BASE-T half duplex is not supported by the link partner |
| 4-0 | Selector | <00000>, RO | Protocol Selection Bits Link partner's binary encoded protocol selector |

8.7 Auto-negotiation Expansion Register (ANER) - 06H

| Bit | Bit Name | Default | Description |
|------|------------|----------|---|
| 15-5 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 4 | PDF | 0, RO/LH | Local Device Parallel Detection Fault PDF = 1: A fault detected via parallel detection function. PDF = 0: No fault detected via parallel detection function |
| 3 | LP_NP_ABLE | 0, RO | Link Partner Next Page Able LP_NP_ABLE = 1: Link partner, next page available LP_NP_ABLE = 0: Link partner, no next page |
| 2 | NP_ABLE | 0,RO/P | Local Device Next Page Able NP_ABLE = 1: DM8203I, next page available NP_ABLE = 0: DM8203I, no next page DM8203I does not support this function, so this bit is always 0 |
| 1 | PAGE_RX | 0, RO | New Page Received A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management |
| 0 | LP_AN_ABLE | 0, RO | Link Partner Auto-negotiation Able A "1" in this bit indicates that the link partner supports Auto-negotiation |

8.8 DAVICOM Specified Configuration Register (DSCR) – 10H

| Bit | Bit Name | Default | Description |
|-----|----------|---------|--|
| 15 | BP_4B5B | 0,RW | Bypass 4B5B Encoding and 5B4B Decoding 1 = 4B5B encoder and 5B4B decoder function bypassed 0 = Normal 4B5B and 5B4B operation |
| 14 | BP_SCR | 0, RW | Bypass Scrambler/Descrambler Function 1 = Scrambler and descrambler function bypassed 0 = Normal scrambler and descrambler operation |
| 13 | BP_ALIGN | 0, RW | Bypass Symbol Alignment Function 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation |
| 12 | Reserved | 0, RO | Reserved |
| 11 | Reserved | RW | Reserved Force to 0 in application |
| 10 | Reserved | 1, RW | Reserved Force to 1 in application. |
| 9 | Reserved | 0, RO | Reserved |
| 8 | Reserved | 0, RW | Reserved Force to 0 in application. |
| 7 | Reserved | 0, RW | Reserved Force to 0 in application. |
| 6 | Reserved | 0, RW | Reserved Force to 0 in application. |



| | | | |
|---|-----------|-------|---|
| 5 | Reserved | 0, RW | Reserved Force to 0 in application. |
| 4 | RPDCTR-EN | 1, RW | Reduced Power Down Control Enable This bit is used to enable automatic reduced power down 0 = Disable automatic reduced power down 1 = Enable automatic reduced power down |
| 3 | SMRST | 0, RW | Reset State Machine When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed |
| 2 | MFPS | 1, RW | MF Preamble Suppression Control MII frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off |
| 1 | SLEEP | 0, RW | Sleep Mode Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset |
| 0 | Reserved | 0, RW | Reserved Force to 0 in application. |

8.9 DAVICOM Specified Configuration and Status Register (DCSR) – 11H

| Bit | Bit Name | Default | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----|-------------|------------|---|---|----|----|----|--|---|---|---|---|---------------|---|---|---|---|---------------|---|---|---|---|-------------------|---|---|---|---|------------------------|---|---|---|---|-------------------|---|---|---|---|------------------------|---|---|---|---|------------------------------------|---|---|---|---|---|---|---|---|---|---|
| 15 | 100FDX | 1, RO | 100M Full Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M full duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | 100HDX | 1, RO | 100M Half Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M half duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13 | 10FDX | 1, RO | 10M Full Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Full Duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | 10HDX | 1, RO | 10M Half Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M half duplex mode. The software can read bit [15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | Reserved | 0, RO | Reserved Read as 0, ignore on write | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | Reserved | 0,RW | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | Reserved | 0,RW | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8-4 | PHYADR[4:0] | 0 or 1, RW | PHY Address Bit 4:0 The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3-0 | ANMB[3:0] | 0, RO | Auto-negotiation Monitor Bits These bits are for debug only. The auto-negotiation status will be written to these bits. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | <table border="1"> <thead> <tr> <th>B3</th> <th>B2</th> <th>B1</th> <th>B0</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>In IDLE state</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Ability match</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>Acknowledge match</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>Acknowledge match fail</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>Consistency match</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>Consistency match fail</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>Parallel detects signal link ready</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>Parallel detects signal link ready fail</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>Auto-negotiation completed successfully</td> </tr> </tbody> </table> | B3 | B2 | B1 | B0 | | 0 | 0 | 0 | 0 | In IDLE state | 0 | 0 | 0 | 1 | Ability match | 0 | 0 | 1 | 0 | Acknowledge match | 0 | 0 | 1 | 1 | Acknowledge match fail | 0 | 1 | 0 | 0 | Consistency match | 0 | 1 | 0 | 1 | Consistency match fail | 0 | 1 | 1 | 0 | Parallel detects signal link ready | 0 | 1 | 1 | 1 | Parallel detects signal link ready fail | 1 | 0 | 0 | 0 | Auto-negotiation completed successfully |
| B3 | B2 | B1 | B0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | In IDLE state | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | Ability match | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | Acknowledge match | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | Acknowledge match fail | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | Consistency match | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | Consistency match fail | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | Parallel detects signal link ready | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | Parallel detects signal link ready fail | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | Auto-negotiation completed successfully | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

8.10 10BASE-T Configuration/Status (10BTCSR) – 12H

| Bit | Bit Name | Default | Description |
|-----|----------|---------|---|
| 15 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 14 | LP_EN | 1, RW | Link Pulse Enable 1 = Transmission of link pulses enabled 0 = Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation |
| 13 | HBE | 1, RW | Heartbeat Enable 1 = Heartbeat function enabled 0 = Heartbeat function disabled When the DM8203I is configured for full duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in full duplex mode) |
| 12 | SQUELCH | 1, RW | Squelch Enable 1 = Normal squelch 0 = Low squelch |
| 11 | JABEN | 1, RW | Jabber Enable Enables or disables the Jabber function when the DM8203I is in 10BASE-T full duplex or 10BASE-T transceiver Loopback mode 1 = Jabber function enabled 0 = Jabber function disabled |
| 10 | SERIAL | 0, RW | 10Mbps Serial Mode (only valid in PHY test mode) Force to 0, in application. |
| 9-1 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 0 | POLR | 0, RO | Polarity Reversed When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed. This bit is automatically set and cleared by 10BASE-T module |

8.11 Power down Control Register (PWDOR) – 13H

| Bit | Bit Name | Default | Description |
|------|----------|---------|--|
| 15-9 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 8 | PD10DRV | 0, RW | Vendor power down control test |
| 7 | PD100DL | 0, RW | Vendor power down control test |
| 6 | PDchip | 0, RW | Vendor power down control test |
| 5 | PDcrm | 0, RW | Vendor power down control test |
| 4 | PDaeq | 0, RW | Vendor power down control test |
| 3 | PDdrv | 0, RW | Vendor power down control test |
| 2 | PDedi | 0, RW | Vendor power down control test |
| 1 | PDedo | 0, RW | Vendor power down control test |
| 0 | PD10 | 0, RW | Vendor power down control test |

* When selected, the power down value is control by Register 14H

8.12 (Specified config) Register – 14H

| Bit | Bit Name | Default | Description |
|-----|----------------|-------------|---|
| 15 | TSTSE1 | 0,RW | Vendor test select 1 control |
| 14 | TSTSE2 | 0,RW | Vendor test select 2 control |
| 13 | Reserved | 0, RO | Reserved |
| 12 | FORCE_FEF | 0,RW | Vendor test select control |
| 11 | PREAMBLEX | 0,RW | Preamble Saving Control 0: when bit 10 is set, the 10BASE-T transmit preamble count is reduced. When bit 11 of register 1DH is set, 12-bit preamble is reduced; otherwise 22-bit preamble is reduced. 1: transmit preamble bit count is normal in 10BASE-T mode |
| 10 | TX10M_PWR | 1,RW | 10BASE-T mode Transmit Power Saving Control 1: enable transmit power saving in 10BASE-T mode 0: disable transmit power saving in 10BASE-T mode |
| 9 | NWAY_PWR | 0,RW | Auto-negotiation Power Saving Control 1: disable power saving during auto-negotiation period 0: enable power saving during auto-negotiation period |
| 8 | Reserved | 0, RO | Reserved Read as 0, ignore on write |
| 7 | MDIX_CNTL | MDI/MDIX,RO | The polarity of MDI/MDIX value 1: MDIX mode 0: MDI mode |
| 6 | AutoNeg_dpbk | 0,RW | Auto-negotiation Loopback 1: test internal digital auto-negotiation Loopback 0: normal. |
| 5 | Mdix_fix Value | 0, RW | MDIX_CNTL force value: When Mdix_down = 1, MDIX_CNTL value depend on the register value. |
| 4 | Mdix_down | 0,RW | MDIX Down Manual force MDI/MDIX. 0: Enable <i>HP</i> Auto-MDIX 1: Disable <i>HP</i> Auto-MDIX , MDIX_CNTL value depend on Reg.14H.bit5 |
| 3 | MonSel1 | 0,RW | Vendor monitor select 1 |
| 2 | MonSel0 | 0,RW | Vendor monitor select 0 |
| 1 | Reserved | 0,RW | Reserved Force to 0, in application. |
| 0 | PD_value | 0,RW | Power down control value Decision the value of each field Reg.13H. 1: power down 0: normal |

8.13 DAVICOM Specified Receive Error Counter Register (RECR) – 16H

| Bit | Bit Name | Default | Description |
|------|-------------|---------|--|
| 15-0 | Rcv_Err_Cnt | 0, RO | Receive Error Counter Receive error counter that increments upon detection of RXER. Clean by read this register. |

8.14 DAVICOM Specified Disconnect Counter Register (DISCR) – 17H

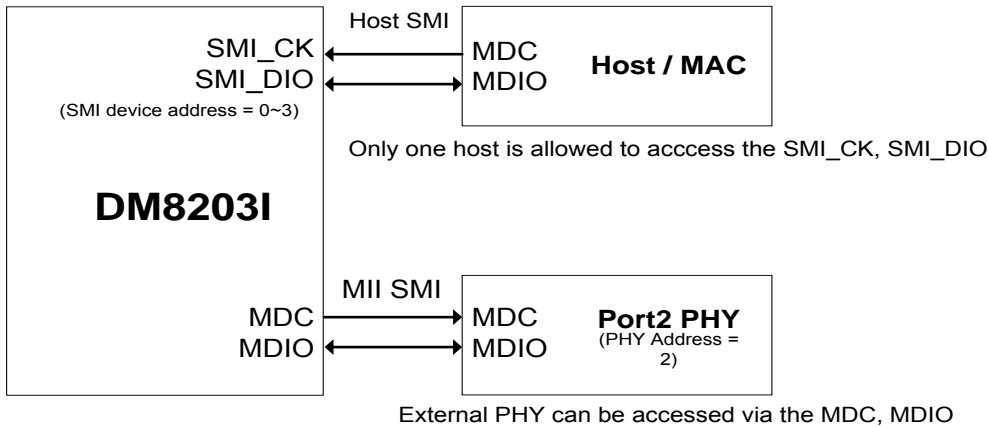
| Bit | Bit Name | Default | Description |
|------|--------------------|---------|---|
| 15-8 | Reserved | 0, RO | Reserved |
| 7-0 | Disconnect Counter | 0, RO | Disconnect Counter that increment upon detection of disconnection. Clean by read this register. |

8.15 Power Saving Control Register (PSCR) – 1DH

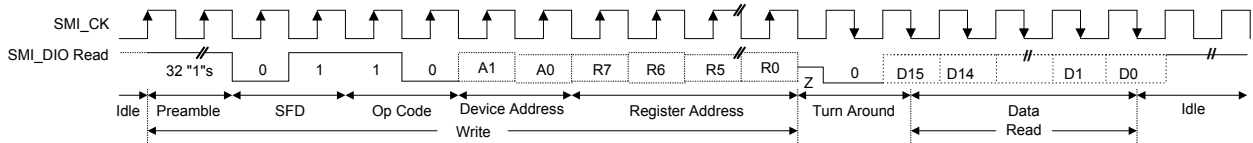
| Bit | Bit Name | Default | Description |
|-------|-----------|---------|---|
| 15-12 | RESERVED | 0,RO | RESERVED |
| 11 | PREAMBLEX | 0,RW | Preamble Saving Control when both bit 10 and 11 of register 14H are set, the 10BASE-T transmit preamble count is reduced. 1: 12-bit preamble is reduced. 0: 22-bit preamble is reduced. |
| 10 | AMPLITUDE | 0,RW | Transmit Amplitude Control Disabled 1: when cable is unconnected with link partner, the TX amplitude is reduced for power saving. 0: disable Transmit amplitude reduce function |
| 9 | TX_PWR | 0,RW | Transmit Power Saving Control Disabled 1: when cable is unconnected with link partner, the driving current of transmit is reduced for power saving. 0: disable transmit driving power saving function |
| 8-0 | RESERVED | 0,RO | RESERVED |

9. Functional Description

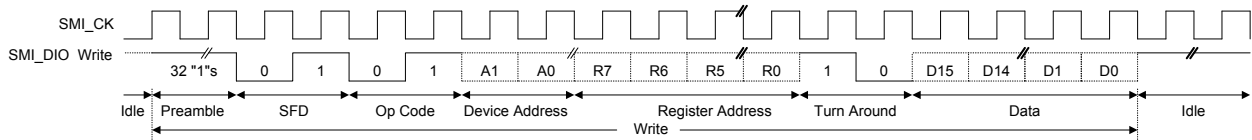
9.1 Serial Management Interface



Host SMI - Read Frame Structure



Host SMI - Write Frame Structure



DM8203I supports two type of serial management interface (SMI), Host SMI and MII SMI. The application of SMI illustrated as below.

1. The Host SMI consists of two pins, one is SMI_CK and another is SMI_DIO. User can access DM8203I's EEPROM, PHY registers, MIB counters and Configuration registers through Host SMI. The format is following. The <Device Address> field of the frame means SMI device address that is configured by strap

pin (TXD2_0 & TXD2_1). The <Register Address> field of the frame is mapped to address of control and status register set of DM8203I. The read/writ data is valid on low byte (D7~D0) of <Data> field, the high byte (D15~D8) of data is reserved.

2. DM8203I supports MII SMI auto-polling for configuring speed, duplex mode, and 802.3x flow control capability of the external PHY (Port2) via the MDC, MDIO. More detail description and frame format can refer to section 9.3.2.

9.2 Switch function:

9.2.1 Address Learning

The DM8203I has a self-learning mechanism for learning the MAC addresses of incoming packets in real time. DM8203I stores MAC addresses, port number and time stamp information in the Hash-based Address Table. It can learn up to 1K unicast address entry.

The switch engine updates address table with new entry if incoming packet's Source Address (SA) does not exist and incoming packet is valid (non-error and legal length).

Besides, DM8203I has an option to disable address learning for individual port. This feature can be set by bit 0 of register 65h

9.2.2 Address Aging

The time stamp information of address table is used in the aging process. The switch engine updates time stamp whenever the corresponding SA receives. The switch engine would delete the entry if its time stamp is not updated for a period of time.

The period can be programmed or disabled through bit 0 & 1 of register 52h.

9.2.3 Packet Forwarding

The DM8203I forwards the incoming packet according to following decision:

(1). If DA is Multicast/Broadcast, the packet is forwarded to all ports, except to the port on which the packet was received.

(2). Switch engine would look up address table based on DA when incoming packets is UNICAST. If the DA was not found in address table, the packet is treated as a multicast packet and forward to other ports. If the DA was found and its destination port number is different to source port number, the packet is forward to destination port.

(3). Switch engine also look up VLAN, Port Monitor setting and other forwarding constraints for the forwarding decision, more detail will discuss in later sections.

The DM8203I will filter incoming packets under following conditions:

(1). Error packets, including CRC errors, alignment errors, illegal size errors.

(2). PAUSE packets.

(3). If incoming packet is UNICAST and its destination port number is equal to source port number.

9.2.4 Inter-Packet Gap (IPG)

IPG is the idle time between any two valid packets at the same port. The typical number is 96 bits time. In other word, the value is 9.6u sec for 10Mbps and 960n sec for 100Mbps.

9.2.5 Back-off Algorithm

The DM8203I implements the binary exponential back-off algorithm in half-duplex mode compliant to IEEE standard 802.3.

9.2.6 Late Collision

Late Collision is a type of collision. If a collision error occurs after the first 512 bit times of data are transmitted, the packet is dropped.

9.2.7 Full Duplex Flow Control

The DM8203I supports IEEE standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, The DM8203I will defer transmitting next normal frames, if it receives a pause frame from link partner.

On the transmit side, The DM8203I issues pause frame with maximum pause time when internal resources such as received buffers, transmit queue and transmit descriptor ring are unavailable. Once resources are available, The DM8203I sends out a pause frame with zero pause time allows traffic to resume immediately.

9.2.8 Half Duplex Flow Control

The DM8203I supports half-duplex backpressure. The inducement is the same as full duplex mode. When flow control is required, the DM8203I sends jam pattern and results in a collision.

The flow control ability can be set in bit 4 of register 61h.

9.2.9 Partition Mode

The DM8203I provides a partition mode for each port, see bit 6 of register 61h. The port enters partition mode when more than 64 consecutive collisions are occurred. In partition mode the port continuous to transmit but it will not receive. The port returned to normal operation mode when a good packet is seen on the wire. The detail description of partition mode represent following:

(1). Entering Partition State

A port will enter the Partition State when either of the following conditions occurs:

- The port detects a collision on every one of 64 consecutive re-transmit attempts to the same packet.
- The port detects a single collision which occurs for more than 512 bit times.
- Transmit defer timer time out, which indicates the transmitting packet is deferred to long.

(2). While in Partition state:

The port will continue to transmit its pending packet, regardless of the collision detection, and will not allow the usual Back-off Algorithm. Additional packets pending for transmission will be transmitted, while ignoring the internal collision indication. This frees up the ports transmit buffers which would otherwise be filled up at the expense of other ports buffers. The assumption is that the partition is signifying a system failure situation (bad connection/cable/station), thus dropping packets is a small price to pay vs. the cost of halting the switch due to a buffer full condition.

(3). Exiting from Partition State

The Port exits from Partition State, following the end of a successful packet transmission. A successful packet transmission is defined as no collisions were detected on the first 512 bits of the transmission.

9.2.10 Broadcast Storm Filtering

The DM8203I has an option to limit the traffic of broadcast or multicast packets, to protect the switch from lower bandwidth availability.

There are two types of broadcast storm control, one is throttling broadcast packet only, the other includes multicast. This feature can be set through bit 1 of register 61h.

The broadcast storm threshold can be programmed by EEPROM or register 67h, the default setting is no broadcast storm protecting.

9.2.11 Bandwidth Control

The DM8203I supports two types of bandwidth control for each port. One is the ingress and egress bandwidth rate can be controlled separately, the other is combined together, this function can be set through bit 3 of register 61h. The bandwidth control is disabled by default.

To separate bandwidth control mode, the threshold rate is defined in register 66h. For combined mode, it is defined in register 67h.

The behavior of bandwidth control as below:

(1).For the ingress control, if flow control function is enabled, Pause or Jam packet will be transmitted. The ingress packets will be dropped if flow control is disabled.

(2).For the egress control, the egress port will not transmit any packets. On the other hand, the ingress bandwidth of source port will be throttled that prevent packets from forwarding.

(3).In combined mode, if the sum of ingress and egress bandwidth over threshold, the bandwidth will be throttled.

9.2.12 Port Monitoring Support

The DM8203I supports "Port Monitoring" function on per port base, detail as below:

(1). Sniffer Port and Monitor Port

There is only one port can be selected as "sniffer port" by register 52h, multiple ports can be set as "receive monitor port" or "transmit monitor port" in per-port register 65h.

(2).Receive monitor

All packets received on the "receive monitor port" are send a copy to "sniffer port". For example, port 0 is set as "receive monitor port" and port 2 is selected as a "sniffer port". If a packet is received from port 0 and predestined to port 1 after forwarding decision, the DM8203I will forward it to port 1 and port 2 in the end.

(3).Transmit monitor

All packets transmitted on the "transmit monitor port" are send a copy to "sniffer port". For example, port 1 is set as "transmit monitor port" and port 2 is selected as "sniffer port". If a packet is received from port 0 and predestined to port 1 after forwarding

decision, the DM8203I will forward it to port 1 and port 2 in the end.

(4).Exception

The DM8203I has an optional setting that broadcast/multicast packets are not monitored (see bit 4 of register 65h). It's useful to avoid unnecessary bandwidth.

- (1). Set PVID of Port 0 to 0x01h.
- (2). Set PVID of Port 1 to 0x02h.
- (3). Set PVID of Port 2 to 0x03h.
- (4). Set register B1h to 0x06h.
- (5). Set register B2h to 0x05h.
- (6). Set register B3h to 0x03h.

9.2.13 VLAN Support

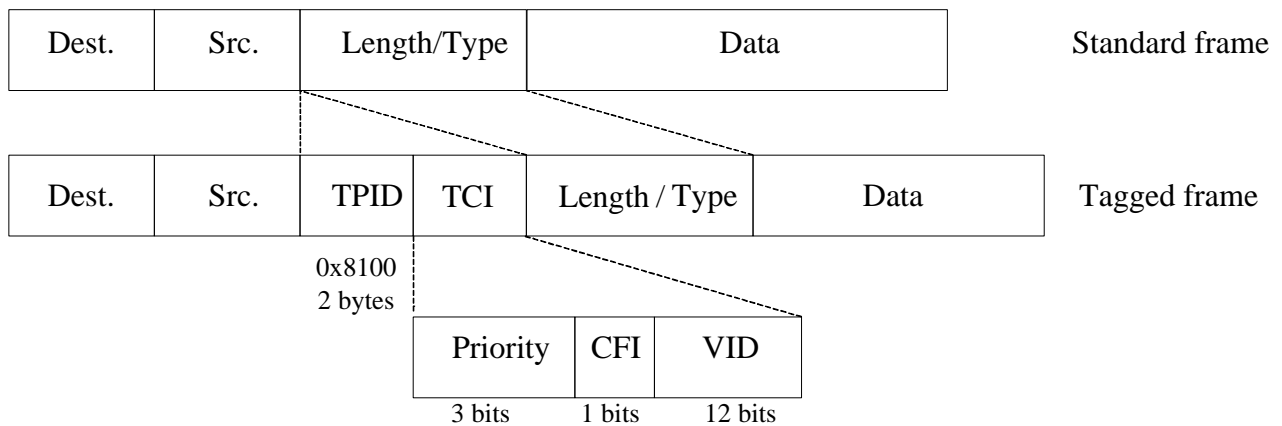
9.2.13.1 Port-Based VLAN

The DM8203I supports port-based VLAN as default, up to 16 groups. Each port has a default VID called PVID (Port VID, see register 6Fh). The DM8203I used LSB 4-bytes of PVID as index and mapped to register B0h~BFh, to define the VLAN groups.

For instance, we intend to partition DM8203I's ports into three groups. Port 0 and port 1 in group A, port 1 and port 2 in group B, finally, port 2 and port 0 in group C. In this case, the setting as below:

9.2.13.2 802.1Q-Based VLAN

Regarding IEEE 802.1Q standard, Tag-based VLAN uses an extra tag to identify the VLAN membership of a frame across VLAN-aware switch/router. A tagged frame is four bytes longer than an untagged frame and contains two bytes of TPID (Tag Protocol Identifier) and two bytes of TCI (Tag Control Information).



The DM8203I also supports 16 802.1Q-based VLAN groups, as specified in bit 1 of register 53h. It's obvious that the tagged packets can be assigned to several different VLANs which are determined according to the VID inside the VLAN Tag. Therefore, the operation is similar to port-based VLAN. The DM8203I used LSB 4-bytes VID of received packet with VLAN tag and VLAN Group Mapping Register (B0h~BFh) to configure the VLAN partition. If the destination port of received packet is not same VLAN group with received port, it will be discarded.

9.2.13.3 Tag/Untag

User can define each port as Tag port or Un-tag port by bit 7 of register 6Dh in 802.1Q-based VLAN mode. The operation of Tag and Un-tag can explain as below conditions:

- (1). Receive untagged packet and forward to Un-tag port.
Received packet will forward to destination port without modification.
- (2). Receive tagged packet and forward to Un-tag port.
The DM8203I will remove the tag from the

packet and recalculate CRC before sending it out.

(3). Receive untagged packet and forward to Tag port.

The DM8203I will insert the PVID tag when an untagged packet enters the port, and recalculate CRC before delivering it.

(4). Receive tagged packet and forward to Tag port.

Received packet will forward to destination port without modification.

9.2.14 Priority Support

The DM8203I supports Quality of Service (QoS) mechanism for multimedia communication such as VoIP and video conferencing.

The DM8203I provides three priority classifications: Port-based, 802.1p-based and DiffServ-based priority. See next section for more detail. The DM8203I offers four level queues for transmit on per-port based.

The DM8203I provides two packet scheduling algorithms: Weighted Fair Queuing and Strict Priority Queuing. Weighted Fair Queuing (WFQ) based on their priority and queue weight. Queues with larger weights get more service than smaller. This mechanism can get highly efficient bandwidth and smooth the traffic. Strict Priority Queuing (SPQ) based on priority only. The Packet on the highest priority queue is transmitted first. The next highest-priority queue is work until last queue empties, and so on. This feature can be set in bit 5 of register 6Dh.

9.2.14.1 Port-Based Priority

Port based priority is the simplest scheme and as default. Each port has a 2-bit priority value as index for splitting ingress packets to the corresponding transmit queue. This value can be set in bit 0 and 1 of register 6Dh.

9.2.14.2 802.1p-Based Priority

802.1p priority can be disabled by bit 2 of register 6Dh, it is enabled by default.

The DM8203I extracts 3-bit priority field from received packet with 802.1p VLAN tag, and maps this field against VLAN Priority Map Registers (D0h~D1h) to determine which transmit queue is designated. The VLAN Priority Map is programmable.

9.2.14.3 DiffServ-Based Priority

DiffServ based priority uses the most significant 6-bit of the ToS field in standard IPv4 header, and maps this field against ToS Priority Map Registers (C0h~CFh) to determine which transmit queue is designated. The ToS Priority Map is programmable too. In addition, User can only refer to most significant 3-bit of the ToS field optionally, see bit 7 of register 53h.

9.3 MII Interface

9.3.1 MII data interface

The DM8203I port 2 provides a Media Independent Interface (MII) as defined in the IEEE 802.3u standard (Clause 22).

The MII consists of a nibble wide receive data bus, a nibble wide transmit data bus, and control signals to facilitate data transfers between the DM8203I port 2 and external device (a PHY or a MAC in reverse MII).

- TXD2 (transmit data) is a nibble (4 bits) of data that are driven by the DM8203I synchronously with respect to TXC2. For each TXC2 period, which TXE2 is asserted, TXD2 (3:0) are accepted for transmission by the external device.
- TXC2 (transmit clock) from the external device is a continuous clock that provides the timing reference for the transfer of the TXE2, TXD2. The DM8203I can drive 25MHz clock if it is configured to reversed MII mode.
- TXE2 (transmit enable) from the DM8203I port 2 MAC indicates that nibbles are being presented on the MII for transmission to the external device.
- RXD2 (receive data) is a nibble (4 bits) of data that are sampled by the DM8203I port 2 MAC synchronously with respect to RXC2. For each RXC2 period which RXDV2 is asserted, RXD2 (3:0) are transferred from the external device to the DM8203I port 2 MAC reconciliation sub layer.
- RXC2 (receive clock) from external device to the DM8203I port 2 MAC reconciliation sub layer is a continuous clock that provides the timing reference for the transfer of the RXDV2, RXD2, and RXER2 signals.
- RXDV2 (receive data valid) input from the external device to indicates that the external device is presenting recovered and decoded nibbles to the DM8203I port 2 MAC reconciliation sub layer. To interpret a receive frame correctly by the reconciliation sub layer, RXDV2 must encompass the frame, starting no later than the Start-of-Frame delimiter and excluding any End-Stream delimiter.
- RXER2 (receive error) input from the external device is synchronously with respect to RXC2. RXER2 will be asserted for 1 or more clock periods to indicate to the reconciliation sub layer that an error

was detected somewhere in the frame being transmitted from the external device to the DM8203I port 2 MAC.

- CRS2 (carrier sense) is asserted by the external device when either the transmit or receive medium is non-idle, and de-asserted by the external device when the transmit and receive medium are idle. The CRS2 can also in output mode when the DM8203I port 2 is configured to reversed MII mode.
- COL2 (collision detection) is asserted by the external device, when both the transmit and receive medium is non-idle, and de-asserted by the external device when the either transmit or receive medium are idle. The COL2 can also in output mode when the DM8203I port 2 is configured to reversed MII mode.

9.3.2 MII Serial Management

The MII serial management interface consists of a data interface, basic register set in DM8203I port 0 and 1, and a serial management interface to the register set. Through this interface it is possible to control and configure multiple PHY devices, include internal two ports, get status and error information, and determine the type and capabilities of the attached PHY device(s). The DM8203I default is polling 3 ports basic registers 0, 1, 4, and 5 to get the link, duplex, and speed status automatically. Alternatively, the DM8203I can be programmed to read or write any registers of 3 ports by section 6.8~11 CSR B, C, D, and E.

The DM8203I management functions correspond to MII specification for IEEE 802.3u-1995 (Clause 22) for registers 0 through 6 with vendor-specific registers 16, 17, 18, 21, 22, 23 and 24~27.

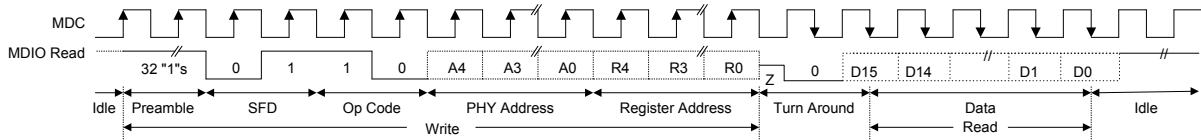
In read/write operation, the management data frame is 64-bits long and starts with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP) : < 10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) filing between Register Address field and Data field is provided for MDIO to avoid contention. Following the turnaround time, 16-bit data is read from or written onto management registers.

9.3.3 Serial Management Interface

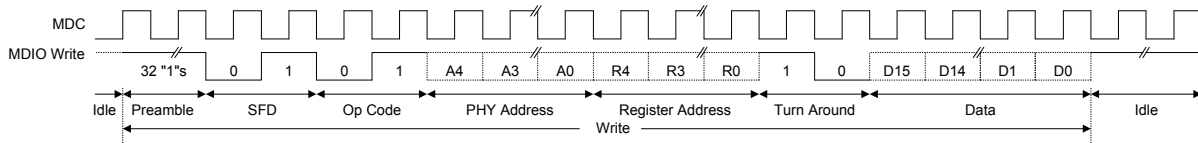
The serial control interface uses a simple two-wired serial interface to obtain and control the status of the physical layer through the MII interface. The serial control interface consists of MDC (Management Data Clock), and MDI/O (Management Data Input/Output) signals.

The MDIO pin is bi-directional and may be shared by up to 32 devices.

9.3.4 Management Interface - Read Frame Structure



9.3.5 Management Interface - Write Frame Structure



9.4 Internal PHY functions

9.4.1 100Base-TX Operation

The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Converter
- NRZI to MLT-3
- MLT-3 Driver

9.4.1.1 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, see reference Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deservations of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating the end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

9.4.1.2 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to the repeated 5B sequences, like the continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

9.4.1.3 Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler, and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI encoder block

9.4.1.4 NRZ to NRZI Encoder

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard, for 100Base-TX transmission over Category-5 unshielded twisted pair cable.

9.4.1.5 MLT-3 Converter

The MLT-3 conversion is accomplished by converting The data stream output, from the NRZI encoder into two binary data streams, with alternately phased logic One event.

9.4.1.6 MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver, which converts these streams to current sources and alternately drives either side of the transmit transformer's primary winding, resulting in a minimal current MLT-3 signal.

9.4.1.7 4B5B Code Group

| Symbol | Meaning | 4B code 3210 | 5B Code 43210 |
|--------|---------|-----------------|------------------|
| 0 | Data 0 | 0000 | 11110 |
| 1 | Data 1 | 0001 | 01001 |
| 2 | Data 2 | 0010 | 10100 |
| 3 | Data 3 | 0011 | 10101 |
| 4 | Data 4 | 0100 | 01010 |
| 5 | Data 5 | 0101 | 01011 |
| 6 | Data 6 | 0110 | 01110 |
| 7 | Data 7 | 0111 | 01111 |
| 8 | Data 8 | 1000 | 10010 |
| 9 | Data 9 | 1001 | 10011 |
| A | Data A | 1010 | 10110 |
| B | Data B | 1011 | 10111 |
| C | Data C | 1100 | 11010 |
| D | Data D | 1101 | 11011 |
| E | Data E | 1110 | 11100 |
| F | Data F | 1111 | 11101 |
| | | | |
| I | Idle | undefined | 11111 |
| J | SFD (1) | 0101 | 11000 |
| K | SFD (2) | 0101 | 10001 |
| T | ESD (1) | undefined | 01101 |
| R | ESD (2) | undefined | 00111 |
| H | Error | undefined | 00100 |
| | | | |
| V | Invalid | undefined | 00000 |
| V | Invalid | undefined | 00001 |
| V | Invalid | undefined | 00010 |
| V | Invalid | undefined | 00011 |
| V | Invalid | undefined | 00101 |
| V | Invalid | undefined | 00110 |
| V | Invalid | undefined | 01000 |
| V | Invalid | undefined | 01100 |
| V | Invalid | undefined | 10000 |
| V | Invalid | undefined | 11001 |

Table 1

9.4.2 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data.

The receive section contains the following functional blocks:

- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

9.4.2.1 Signal Detect

The signal detects function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX standards for both voltage thresholds and timing parameters.

9.4.2.2 Adaptive Equalization

When transmitting data over copper twisted pair cable at high speed, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation, caused by frequency variations, must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation, which will be over-killed in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

9.4.2.3 MLT-3 to NRZI Decoder

The DM8203I decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data.

9.4.2.4 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125 MHz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ decoder.

9.4.2.5 NRZI to NRZ

The transmit data stream is required to be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

9.4.2.6 Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter. It converts the data stream to parallel data to be presented to the descrambler.

9.4.2.7 Descrambler

Because of the scrambling process requires to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, and it descrambles the data streams, and presents the data streams to the Code Group alignment block.

9.4.2.8 Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected and subsequent data is aligned on a fixed boundary.

9.4.2.9 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups receive the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R Symbols).

The T/R symbol pair is also stripped from the nibble, presented to the Reconciliation layer.

9.4.3 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM8203I is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented in nibble format, converted to a serial bit stream, then the Manchester encoded. When receiving, the bit stream, encoded by the Manchester, is decoded and converted into nibble format.

9.4.4 Collision Detection

For half-duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. Collision detection is disabled in full duplex operation.

9.4.5 Carrier Sense

Carrier Sense (CRS) is asserted in half-duplex operation during transmission or reception of data. During full-duplex mode, CRS is asserted only during Receive operations.

9.4.6 Auto-Negotiation

The objective of Auto-negotiation is to provide a means to exchange information between linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-negotiation does not test the characteristics of the linked segment. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

Auto-negotiation also provides a parallel detection function for devices that do not support the Auto-negotiation feature. During Parallel detection there is no exchange of information of configuration. Instead, the receive signal is examined. If it is discovered that the signal matches a technology, which the receiving device supports, a connection will be automatically established using that technology. This allows devices not to support Auto-negotiation but support a common mode of operation to establish a link.

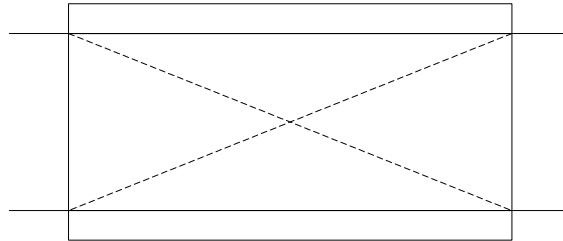
9.5 HP Auto-MDIX Functional Descriptions

The DM8203I supports the automatic detect cable connection type, MDI/MDIX (straight through/cross over). A manual configuration by register bit for MDI or MDIX is still accepted.

When set to automatic, the polarity of MDI/MDIX controlled timing is generated by 16-bits LFSR. The switching cycle time is located from 200ms to 420ms. The polarity control is always switch until detect received signal. After selected MDI or MDIX, This feature is able to detect the required cable connection type. (Straight through or crossed over) and make correction automatically

RX +/- from DM8203I

RX+/- to RJ45



TX +/- from DM8203I

TX+/- to RJ45

* MDI: _____

* MDIX: - - - - -

10. DC and AC Electrical Characteristics

10.1 Absolute Maximum Ratings (-40°C ~ +85°C)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|------------------|---|------|------|------|------------------|
| VCC3 | 3.3V Supply Voltage | -0.3 | 3.6 | V | |
| VCCI | 1.8V core power supply | -0.3 | 1.95 | V | |
| AVDD3 | Analog power supply 3.3V | -0.3 | 3.6 | V | |
| AVDDI | Analog power supply 1.8V | -0.3 | 1.95 | V | |
| V _{IN} | DC Input Voltage (VIN) | -0.5 | 5.5 | V | |
| T _{STG} | Storage Temperature range | -65 | +150 | °C | |
| T _A | Ambient Temperature | -40 | +85 | °C | |
| L _T | Lead Temperature (TL, soldering, 10 sec.). | - | +260 | °C | Lead-free Device |

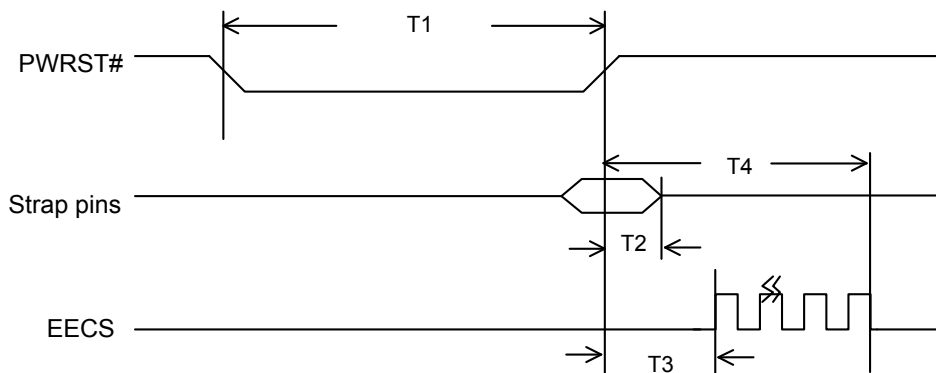
10.2 Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|--|-------------------------------|-------|------|-------|-----------|--------------------------------|
| VCC3 | 3.3V Supply Voltage | 3.135 | - | 3.465 | V | - |
| VCCI | 1.8V core power supply | 1.71 | - | 1.89 | V | - |
| AVDD3 | Analog power supply 3.3V | 3.135 | - | 3.465 | V | - |
| AVDDI | Analog power supply 1.8V | 1.71 | - | 1.89 | V | - |
| P _D (Power Dissipation) | 100BASE-TX | - | 230 | - | mA | 1.8V only |
| | | - | 70 | - | mA | 3.3V only |
| | 10BASE-TX | - | 140 | - | mA | TX idle, 1.8V only |
| | | - | 250 | - | mA | 50% utilization, 1.8V only |
| | | - | 360 | - | mA | 100% utilization, 1.8V only |
| | Auto-negotiation or cable off | - | 30 | - | mA | 3.3V only |
| | | - | 170 | - | mA | 1.8V only |
| | - | 40 | - | mA | 3.3V only | |

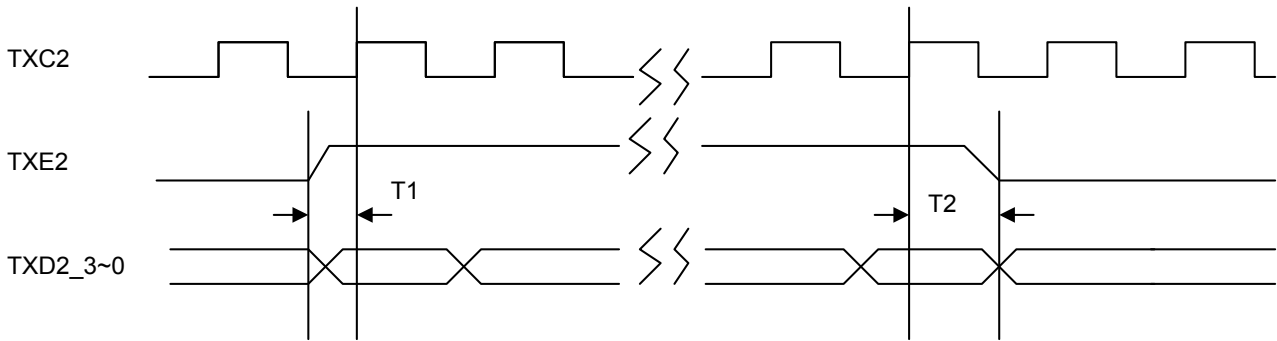
10.3 DC Electrical Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|--------------------|--------------------------------------|------|------|------|------|---------------------------------|
| Inputs | | | | | | |
| VIL | Input Low Voltage | - | - | 0.8 | V | Vcond1 |
| VIH | Input High Voltage | 2.0 | - | - | V | Vcond1 |
| IIL | Input Low Leakage Current | -1 | - | - | uA | VIN = 0.0V, Vcond1 |
| IIH | Input High Leakage Current | - | - | 1 | uA | VIN = 3.3V, Vcond1 |
| Outputs | | | | | | |
| VOL | Output Low Voltage | - | - | 0.4 | V | IOL = 4mA |
| VOH | Output High Voltage | 2.4 | - | - | V | IOH = -4mA |
| Receiver | | | | | | |
| VICM | RX+/RX- Common Mode Input Voltage | - | 1.8 | - | V | 100 Ω Termination Across |
| Transmitter | | | | | | |
| VTD100 | 100TX+/- Differential Output Voltage | 1.9 | 2.0 | 2.1 | V | Peak to Peak |
| VTD10 | 10TX+/- Differential Output Voltage | 4.4 | 5 | 5.6 | V | Peak to Peak |
| ITD100 | 100TX+/- Differential Output Current | 19 | 20 | 21 | mA | Absolute Value |
| ITD10 | 10TX+/- Differential Output Current | 44 | 50 | 56 | mA | Absolute Value |

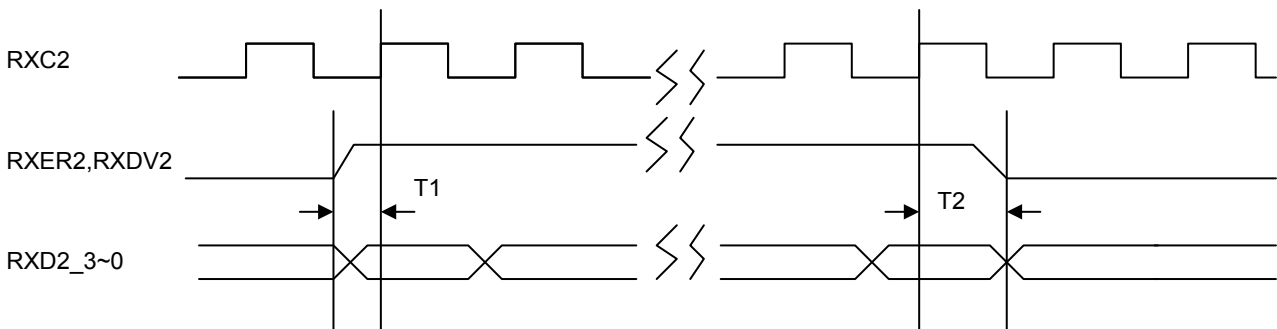
Note: Vcond1 = VCC3 = 3.3V, VCCI = 1.8V, AVDD3 = 3.3V, AVDDI = 1.8V.

10.4 AC characteristics
10.4.1 Power On Reset Timing


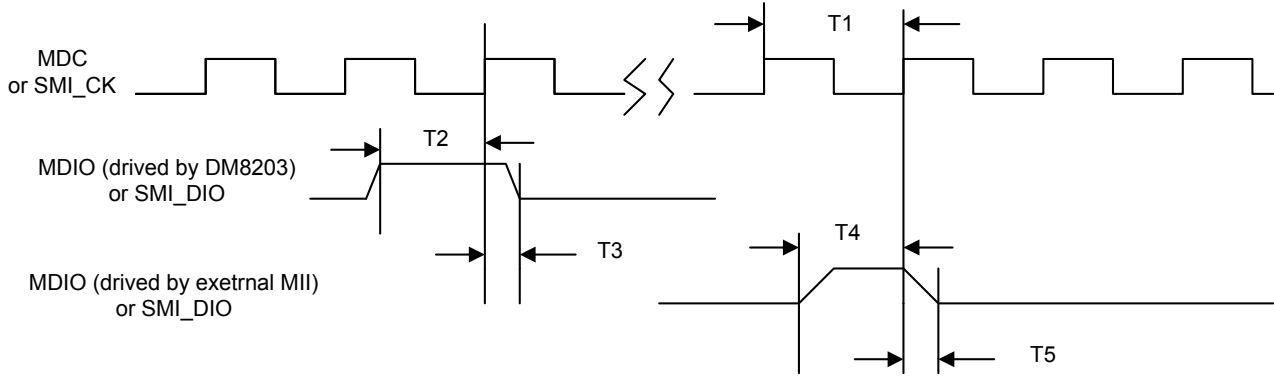
| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|--------|---------------------------------|------|------|------|------|------------|
| T1 | PWRST# Low Period | 1 | - | - | ms | - |
| T2 | Strap pin hold time with PWRST# | 40 | - | - | ns | - |
| T3 | PWRST# high to EECS high | - | 5 | - | us | |
| T4 | PWRST# high to EECS burst end | - | -- | 4 | ms | |

10.4.2 Port 2 MII Interface Transmit Timing


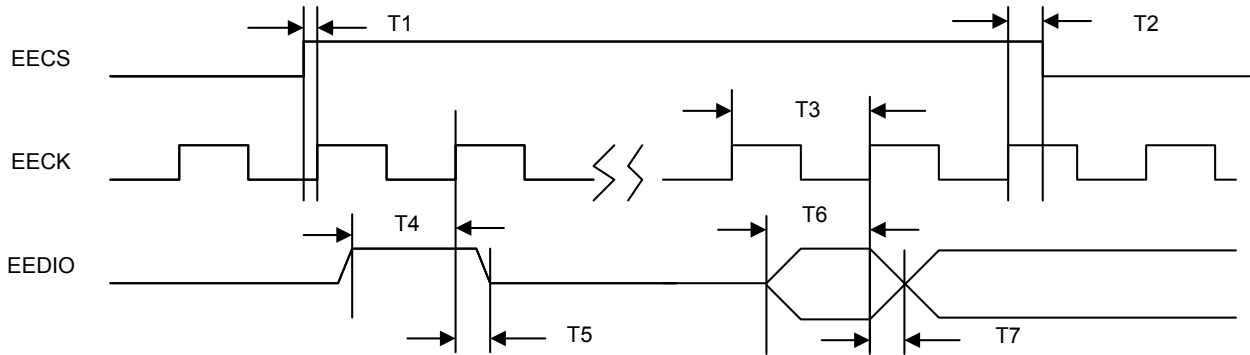
| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|---------------------------|------|------|------|------|
| T1 | TXE2, TXD2_3~0 Setup Time | | 32 | | ns |
| T2 | TXE2, TXD2_3~0 Hold Time | | 8 | | ns |

10.4.3 Port 2 MII Interface Receive Timing


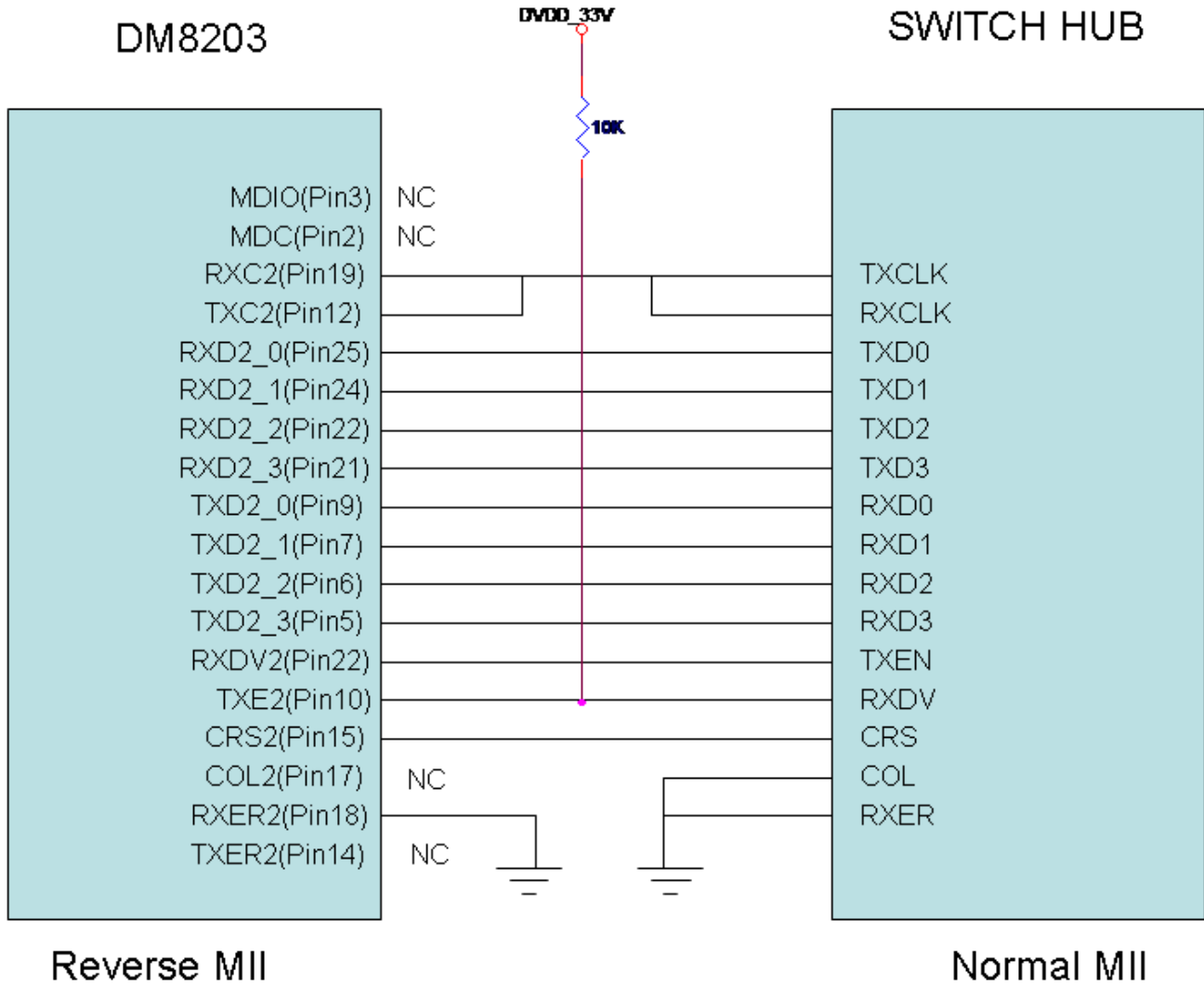
| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|-----------------------------------|------|------|------|------|
| T1 | RXER2, RXDV2, RXD2_3~0 Setup Time | 5 | | | ns |
| T2 | RXER2, RXDV2, RXD2_3~0 Hold Time | 5 | | | ns |

10.4.4 MII Management or host SMI Interface Timing


| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|--|------|------|------|------|
| T1 | MDC or SMI_CK Frequency | | 0.52 | | MHz |
| T2 | MDIO or SMI_DIO by DM8203I Setup Time | | 955 | | ns |
| T3 | MDIO or SMI_DIO by DM8203I Hold Time | | 960 | | ns |
| T4 | MDIO or SMI_DIO by External MII Setup Time | 40 | | | ns |
| T5 | MDIO or SMI_DIO by External MII Hold Time | 40 | | | ns |

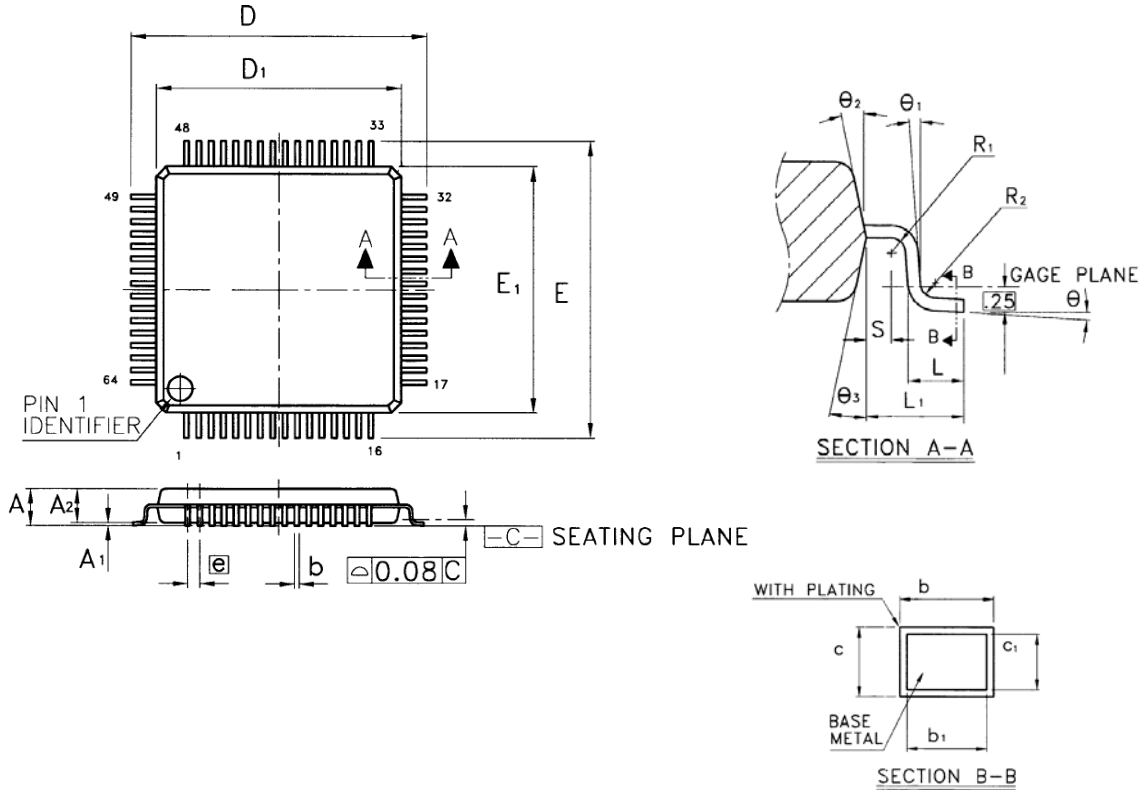
10.4.5 EEPROM timing


| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|----------------------------------|------|------|------|------|
| T1 | EECS Setup Time | | 480 | | ns |
| T2 | EECS Hold Time | | 2080 | | ns |
| T3 | EECK Frequency | | 0.38 | | MHz |
| T4 | EEDIO Setup Time in output state | | 460 | | ns |
| T5 | EEDIO Hold Time in output state | | 2100 | | ns |
| T6 | EEDIO Setup Time in input state | 8 | | | ns |
| T7 | EEDIO Hold Time in input state | 8 | | | ns |

11.2 Application of Reverse MII

Application of Reverse MII

12. Package Information

64 Pins LQFP Package Outline Information:



| Symbol | Dimension in mm | | | Dimension in inch | | |
|----------------|-----------------|------|------|-------------------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | - | - | 1.60 | - | - | 0.063 |
| A ₁ | 0.05 | - | 0.15 | 0.002 | - | 0.006 |
| A ₂ | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.009 | 0.011 |
| b ₁ | 0.17 | 0.20 | 0.23 | 0.007 | 0.008 | 0.009 |
| c | 0.09 | - | 0.20 | 0.004 | - | 0.008 |
| c ₁ | 0.09 | - | 0.16 | 0.004 | - | 0.006 |
| D | 12.00 BSC | | | 0.472 BSC | | |
| D ₁ | 10.00 BSC | | | 0.394 BSC | | |
| E | 12.00 BSC | | | 0.472 BSC | | |
| E ₁ | 10.00 BSC | | | 0.394 BSC | | |
| e | 0.50 BSC | | | 0.020 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L ₁ | 1.00 REF | | | 0.039 REF | | |
| R ₁ | 0.08 | - | - | 0.003 | - | - |
| R ₂ | 0.08 | - | 0.20 | 0.003 | - | 0.008 |
| S | 0.20 | - | - | 0.008 | - | - |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ ₁ | 0° | - | - | 0° | - | - |
| θ ₂ | 12° TYP | | | 12° TYP | | |
| θ ₃ | 12° TYP | | | 12° TYP | | |

1. Dimension D₁ and E₁ do not include resin fin.
2. All dimensions are base on metric system.
3. General appearance spec should base on its final visual inspection spec.



13. Ordering Information

| Part Number | Pin Count | Package |
|-------------|-----------|-------------------|
| DM8203IEP | 64 | LQFP (Pb-free) |

Disclaimer

The information appearing in this publication is believed to be accurate. Integrated circuits sold by DAVICOM Semiconductor are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. DAVICOM makes no warranty, express, statutory, implied or by description regarding the information in this publication or regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHER, DAVICOM MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. DAVICOM reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by DAVICOM for such applications. Please note that application circuits illustrated in this document are for

reference purposes only.

DAVICOM's terms and conditions printed on the order acknowledgment govern all sales by DAVICOM. DAVICOM will not be bound by any terms inconsistent with these unless DAVICOM agrees otherwise in writing. Acceptance of the buyer's orders shall be based on these terms.

Company Overview

DAVICOM Semiconductor Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.

Contact Windows

For additional information about DAVICOM products, contact the Sales department at:

Headquarters

Hsin-chu Office:

No.6 Li-Hsin Rd. VI,
Science-based Park,
Hsin-chu City, Taiwan, R.O.C.
TEL: +886-3-5798797
FAX: +886-3-5646929
MAIL: sales@davicom.com.tw
HTTP: <http://www.davicom.com.tw>

WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.