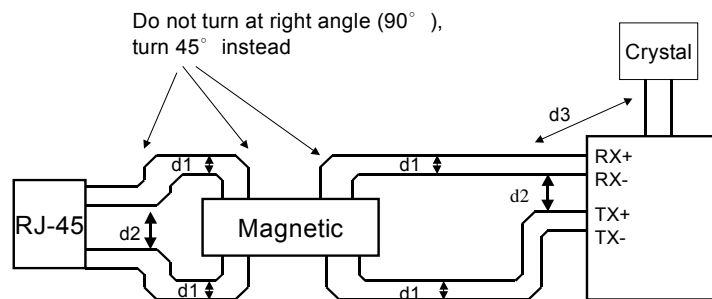


1. Placement, Signal and Trace Routing

- Place the 10/100M magnetic as close as possible to the DM9000 (no more than 20mm) and to the RJ-45 connector.
- Place the termination resistors 50Ω as close as possible to the 10/100M magnetic and the DM9000 RX \pm pins and TX \pm pins. The 50Ω resistors and grounding capacitors of TX \pm and RX \pm should be placed near the DM9000 (no more than 10mm).
- The 25MHz crystal should not be placed near important signal traces, such as RX \pm receive pair and TX \pm transmit pair, band gap resistor, magnetic, and board edge.
- Traces routed from the DM9000 RX \pm pair to the 10/100M magnetic and the RJ45 connector should run symmetrically, directly, identically, and closely (no more than 2mm). The same rule is applied to traces routed from the DM9000 TX \pm pair.

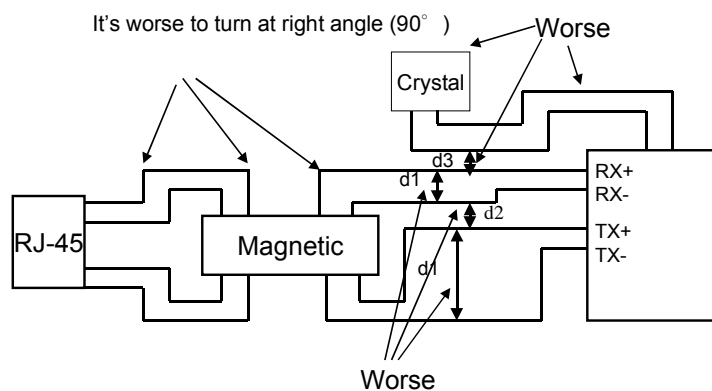


better

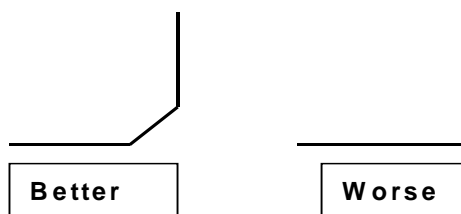
$d1 < 2\text{mm}$

$d2 > 3\text{mm}$; having AGND as a shield is better

$d3 > 5\text{mm}$; having AGND as a shield is better



- It is recommended that RX \pm receive and TX \pm transmit traces turn at 45° angle or in arc. Do not turn at right angle.



- Avoid using vias in routing the traces of RX \pm pair and TX \pm pair.
- The RX \pm pair, TX \pm pair, clock, and power traces should be as short and wide as possible.
- Do not place the DM9000 RX \pm receive pair across the TX \pm transmit pair. Keep the receive pair away from the transmit pair (no less than 3mm). It's better to place ground plane between these two pairs of traces.
- The network interface (see Figure 3-1 and Figure 4) does not route any digital signal between the DM9000 RX \pm and TX \pm pairs to the RJ-45. Keep the two pairs away from all the other active signals and the chassis ground.
- It should be no power or ground plane in the area under the network side of the 10/100M magnetic and the area under the RJ-45 connector.
- Any terminated pins of the RJ-45 connector (pins 4,5,7 and 8, see Figure 1) and the magnetic (see Figure 1) should be tied as closely as possible to the chassis ground through a resistor divider network 75 Ω resistors (no more than 2mm to the magnetic) and a 0.01 μ F/2KV bypass capacitor.
- The Band Gap resistor should be placed as close as possible to pins 26 and 25 (BGRES, AGND) (no more than 3mm). Avoid running any high-speed signal near the Band Gap resistor placement (no less than 3mm from 25MHz X1 and X2).

10Base-T/100Base-TX Application

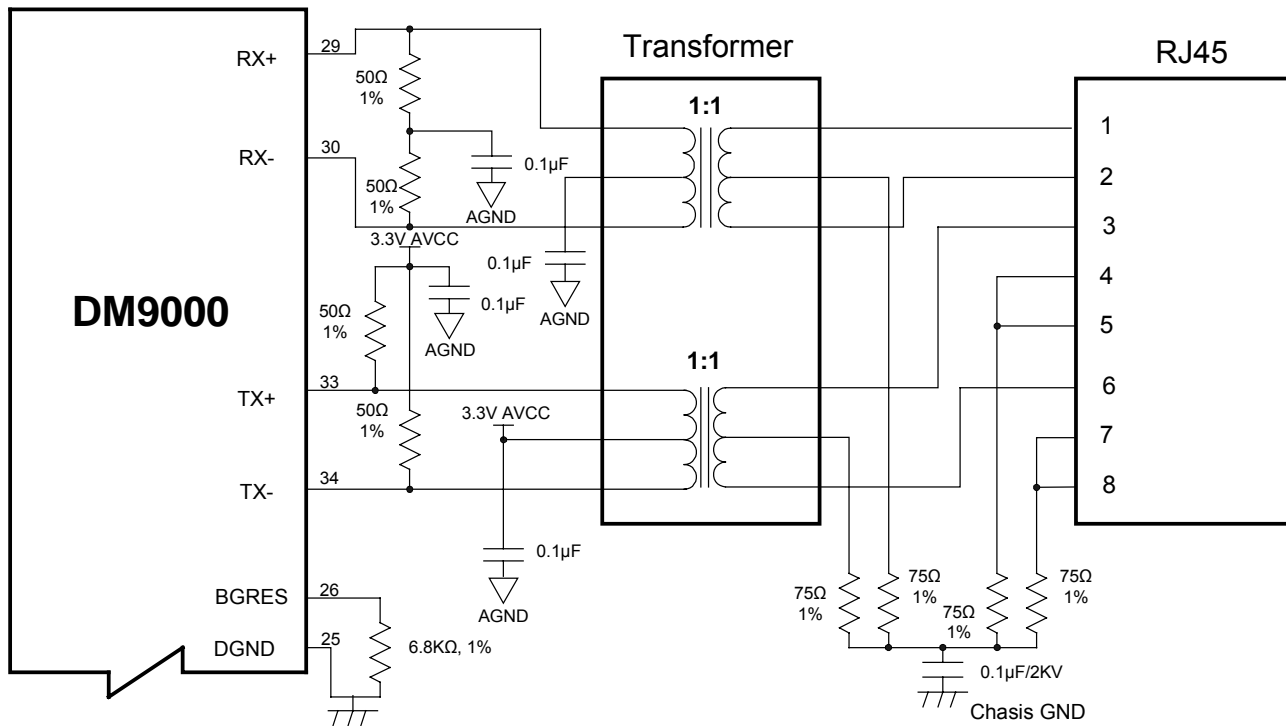


Figure 1

2. Power Supply Decoupling Capacitors

- Place all the decoupling capacitors for all the power supply pins as close as possible to the power pads of the DM9000 (no more than 2.5mm from the above mentioned pins). The recommended decoupling capacitor is 0.1 μ F or 0.01 μ F.
- The PCB layout and power supply decoupling should provide sufficient decoupling to achieve the following when measured at the device:
 - (1) All DVDDs and AVDDs should be within 50m Vpp of each other,
 - (2) All DGNDs and AGNDs should be within 50m Vpp of each other.
 - (3) The resultant AC noise voltage measured across each DVDD/DGND set and AVDD/AGND set should be less than 100m Vpp.
- The 0.1-0.01 μ F decoupling capacitor should be connected between each DVDD/DGND set and AVDD/AGND set be placed as close as possible to the pins of DM9000. The conservative approach is to use two decoupling capacitors on each DVDD/DGND set and AVDD/AGND set. One 0.1 μ F is for low frequency noise, and the other 0.01 μ F is for high frequency noise on the power supply.
- The AVDD connection to the transmit center tap of the magnetic has to be well decoupled to minimize common mode noise injection from the power supply into the twisted pair cable. It is recommended that a 0.01 μ F decoupling capacitor should be placed between the center tap AVDD to AGND ground plane. This decoupling capacitor should be placed as close as possible to the center tap of the magnetic.

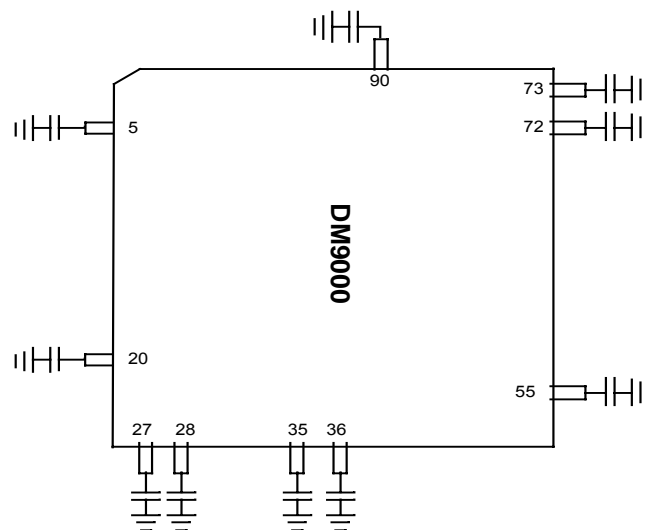


Figure 2

3. Ground Plane Layout

- Place a single ground plane approach to minimize EMI. Ground plane partitioning can cause increased EMI emissions that could make the network interface card (NIC) not comply with specific FCC part 15 and CE regulations.
- Ground plane need separate analog ground domain and digital ground domain. The analog ground domain and digital ground domain connected line is far away from the AGND pins of DM9000 (see Figure 3-1).
- All AGND pins (pin 25, 31, 32, 76) could not directly short each other (see Figure 3-3). It must be directly connected to analog ground domain (see Figure 3-2).
- Analog ground domain area is as large as possible

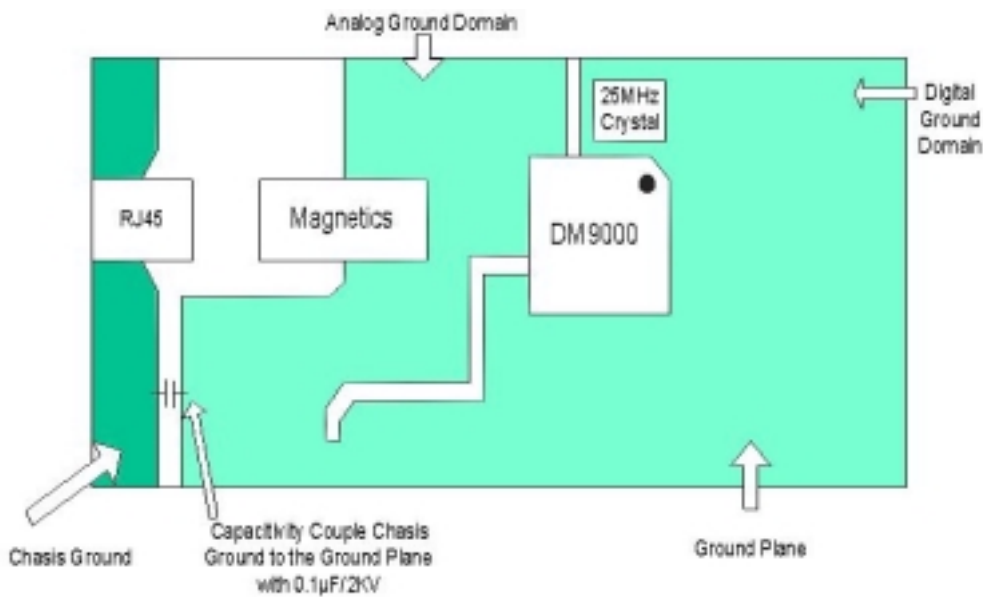


Figure 3-1

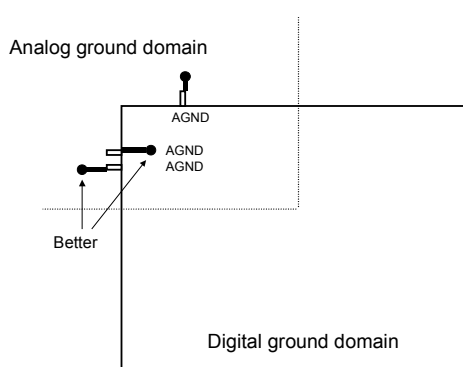


Figure 3-2

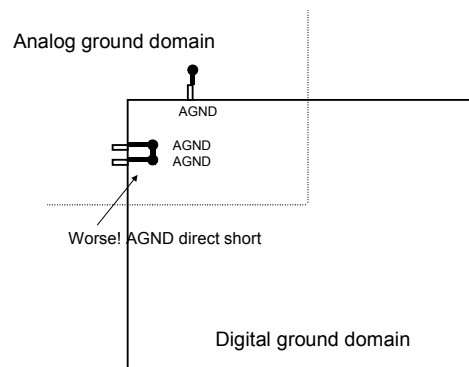


Figure 3-3

4. Power Plane Partitioning

- The power planes should be approximately illustrated in Figure 4. The ferrite bead used should have an impedance 100Ω at 100MHz and 250mA above. A suitable bead is the Panasonic surface mount bead, part number EXCCL4532U or an equivalent. A $10\mu\text{F}$, $0.1\mu\text{F}$ and $0.01\mu\text{F}$ electrolytic bypass capacitors should be connected between VDD and GND at the device side of each of the ferrite bead.
- Separate analog power planes from noisy logic power planes.

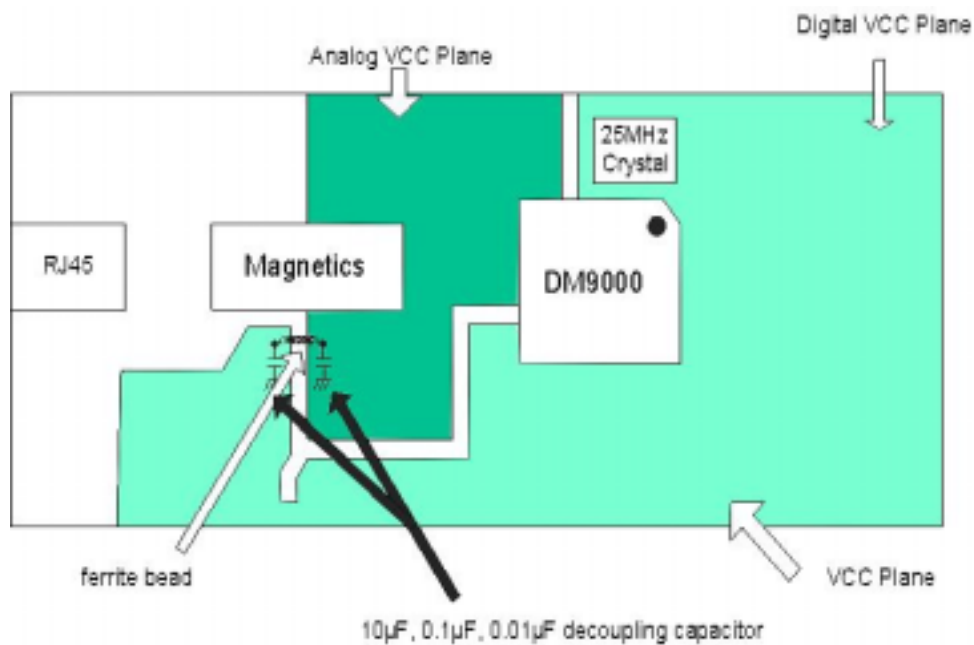


Figure 4

5. Magnetics Selection Guide

- Refer to the following tables 5-1 and 5-2 for 10/100M magnetic sources and specification requirements. The magnetics which meet these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetic specifications before using them in an application. The magnetics listed in the following table are electrical equivalents, but may not be pin-to-pin equivalents.

Manufacturer	Part Number
Pulse Engineering	PE-68515, H1078, H1012, H1102
Delta	LF8200, LF8221x
YCL	20PMT04, 20PMT05
Halo	TG22-3506ND, TG22-3506G1, TG22-S010ND TG22-S012ND
Nano Pulse Inc.	NPI 6181-37, NPI 6120-30, NPI 6120-37, NPI 6170-30
Fil-Mag	PT41715
Bel Fuse	S558-5999-01
Valor	ST6114, ST6118
Macronics	HS2123, HS2213

Table 5-1: 10/100M Magnetic Sources

Parameter	Values	Units	Test Condition
Tx / RX turns ratio	1:1 CT / 1:1	-	-
Inductance	350	μH (Min)	-
Insertion loss	1.1	dB (Max)	1 – 100 MHz
Return loss	-18	dB (Min)	1 – 30 MHz
	-14	dB (Min)	30 – 60 MHz
	-12	dB (Min)	60 – 80 MHz
Differential to common mode rejection	-40	dB (Min)	1 – 60 MHz
	-30	dB (Min)	60 – 100 MHz
Transformer isolation	1500	V	-

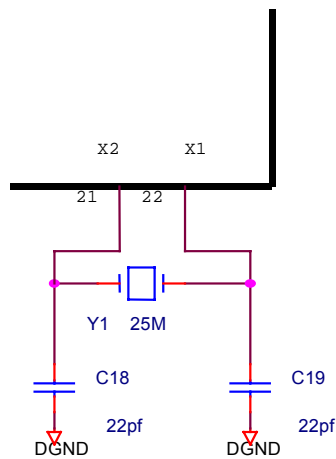
Table 5-2: Magnetic Specification Requirements

6. Crystal Selection Guide

- A crystal can be used to generate the 25MHz reference clock instead of an oscillator. The crystal must be a fundamental type, series-resonant, connect to X1 and X2, and shunt each crystal lead to ground with a 22pF capacitor as shown in Figure 6.

PARAMETER	SPEC
Type	Fundamental, series-resonant
Frequency	25 MHz +/- 0.01%
Equivalent Series Resistance	25 ohms max
Load Capacitance	22 pF typ.
Case Capacitance	7 pF max.
Power Dissipation	1mW max.
Frequency Tolerance (25°C)	30 ppm max.

Table 6-1: Crystal Specifications



**Figure 6
Crystal Circuit Diagram**