DM9000B WoL under 16-bit Mode

Application Note

Version: V01

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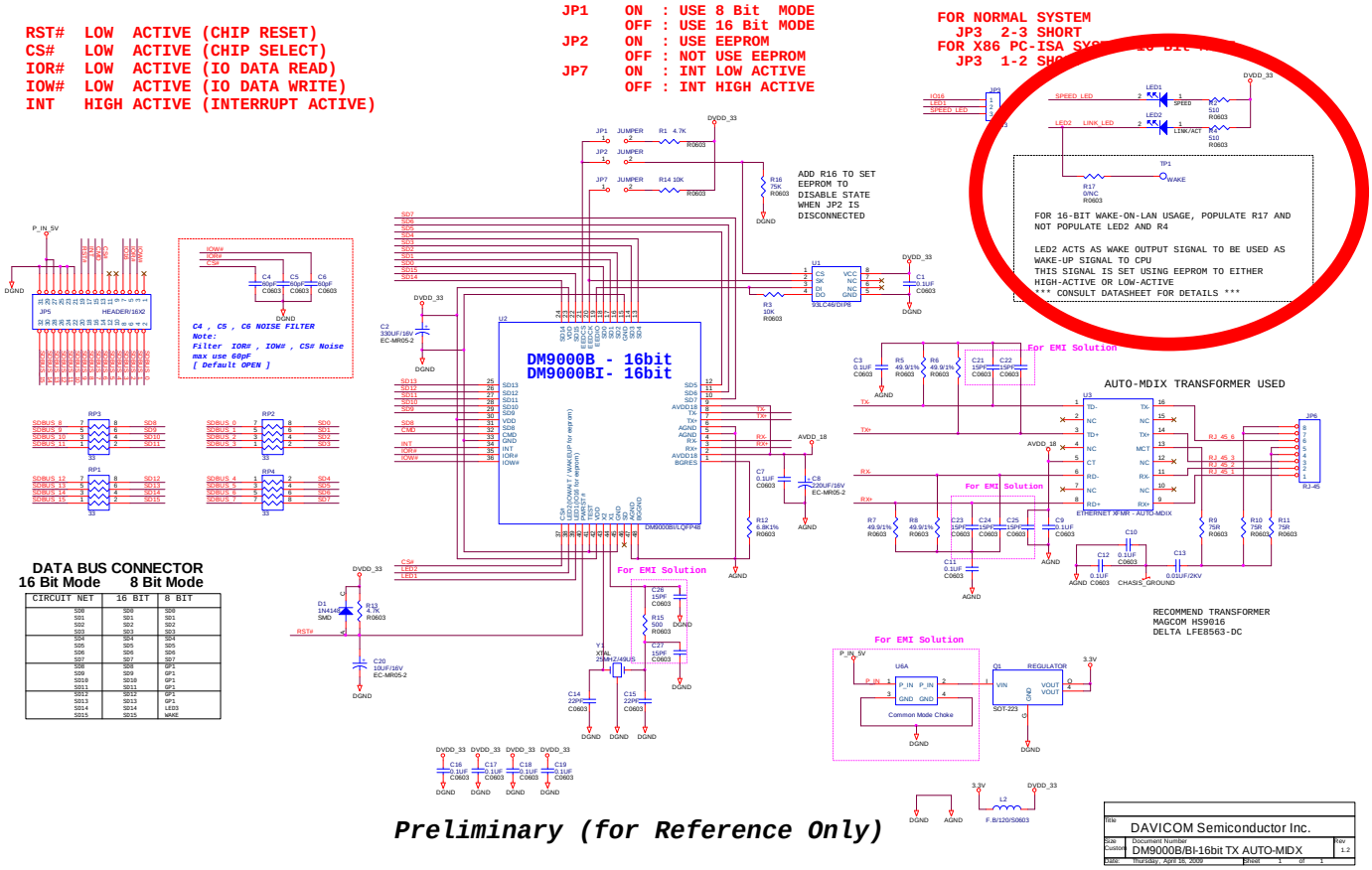
● Hardware

To implement DM9000B WoL (Wake on LAN) function under 16-bit mode, please refer to the following circuit, particularly highlighted by red circle. Resistor R17 must be added and meanwhile LED2 and Resistor R4 must be removed. That means the Pin38 will support WOL function so that LED2 (Link/ACT) function is sacrifice.



● WOL Programming

There are three methods to generate WOL signals: the Magic Packet, the Link Change, and the Sample Frame types.

```
/*
** Enable Wake-up on LAN
*/
#define DM9_NCR     0x00
#define DM9_WCR    0x0F

static void dm9_WOL_enable (board_info_t *db)
{
  u8 tmp;

// Magic Packet event enable
  tmp = (ior(db,DM9_WCR)| 0x08);
  iow(db,DM9_WCR,tmp);
  tmp = (ior(db,DM9_NCR)| 0x40); /* Wake-up function enable */
  iow(db,DM9_NCR,tmp);
}
```

Magic Packet

If the DM9000A/B receives a broadcast packet which content is "FF:FF:FF:FF:FF:FF" + "16 times of Ethernet node address", then the wake-up pin will be activated. Please note that the individual Ethernet node address must be the same as the unicast address in the PAR REG. 10H ~ REG. 15H.

For example:

```
#define NCR 0x00
#define WCR 0x0F
iow ( WCR, ior ( WCR ) | 0x08 ); /* Magic Packet event enable */
iow ( NCR, ior ( NCR ) | 0x40 ); /* Wake-up remote enable */

/* If Ethernet node address in PAR REG. 10H ~ REG. 15H is 00:60:6e:90:00:01 */
/* DM9000A WOL would be active, while received the Magic packet as follows, */
/* FF FF FF FF FF FF 00 60 6E 90 00 01 00 60 6E 90 00 01 00 60 6E 90 00 01 */
/* 00 60 6E 90 00 01 00 60 6E 90 00 01 00 60 6E 90 00 01 00 60 6E 90 00 01 */
/* 00 60 6E 90 00 01 00 60 6E 90 00 01 00 60 6E 90 00 01 00 60 6E 90 00 01 */
/* 00 60 6E 90 00 01 00 60 6E 90 00 01 00 60 6E 90 00 01 00 60 6E 90 00 01 */
/* 00 60 6E 90 00 01 (+ another DM9000A TX 4-byte CRC auto appends) */
```

● DM9000B WOL test on 16bit mode (EEPROM Setting)

In addition to WOL Programming, it needs to be added the following EEPROM setting.

EEPROM Format

name	Word	offset	Description
MAC address	0	0~5	6 Byte Ethernet Address
Auto Load Control	3	6-7	Bit 1:0=01: Update vendor ID and product ID Bit 3:2=01: Accept setting of WORD6 [8:0] Bit 5:4=01: reserved Bit 7:6=01: Accept setting of WORD7 [3:0] (in 8-bit mode) Bit 9:8=01: reserved Bit 11:10=01: Accept setting of WORD7 [7] Bit 13:12=01: Accept setting of WORD7 [8] Bit 15:14=01: Accept setting of WORD7 [15:12]
Vendor ID	4	8-9	2 byte vendor ID (Default: 0A46H)
Product ID	5	10-11	2 byte product ID (Default: 9000H)
Pin control	6	12-13	When word 3 bit [3:2]=01, these bits can control the CS#, IOR#, IOW# and INT pins polarity. Bit0: CS# pin is active low when set (default active low) Bit1: IOR# pin is active low when set (default: active low) Bit2: IOW# pin is active low when set (default: active low) Bit3: INT pin is active low when set (default: active high) Bit4: INT pin is open-collected (default: force output) Bit 15:5: Reserved
Wake-up mode control	7	14-15	Bit0: The WAKE pin is active low when set (default: active high) Bit1: The WAKE pin is in pulse mode when set (default: level mode) Bit2: magic wakeup event is enabled when set. (default: disable) Bit3: link change wakeup event is enabled when set (default disable) Bit6:4: reserved Bit7: LED mode 1 (default: mode 0) Bit8: internal PHY is enabled after power-on (default: disable) Bit11:9: reserved Bit13:12:00 or 11 for normal LED function Bit13:12: 01 (reserved for test only) Bit13:12: 10 LED2 act as WAKE in 16-bit mode Bit14: 1: HP Auto-MDIX ON, 0: HP Auto-MDIX OFF(default ON) Bit 15: 0: LED1 normal function 1: reserved for test only

1. **WOL when link change, pulse mode, high active.**
   a. EEPROM setting
      WORD 3 => 0x5555
      WORD 7 => 0x610A
   b. Result
      i. MAC register

MAC Register	Before	After
0FH	0x20	0x24

      ii. Pin 38 (LED2 as wake up pin)
2. **WOL when magic packet received, pulse mode, high active.**
   a. EEPROM setting
      WORD 3 => 0x5555
      WORD 7 => 0x6106
   b. MAC register setting
      05H => 0x0F
   c. Result
      i. MAC register

MAC Register	Before	After
0FH	0x08	0x09

      ii. Pin 38 (LED2 as wake up pin)
3. **WOL when link change, level mode, low active.**
   a. EEPROM setting
      WORD 3 => 0x5555
      WORD 7 => 0x6109
   b. Result
      i. MAC register

MAC Register	Before	After
0FH	0x20	0x24

      ii. Pin 38 (LED2 as wake up pin)
4. **WOL when magic packet received, level mode, low active.**
   a. EEPROM setting
      WORD 3 => 0x5555
      WORD 7 => 0x6105
   b. MAC register setting
      05H => 0x0F
   c. Result
      i. MAC register

MAC Register	Before	After
0FH	0x08	0x09

      ii. Pin 38 (LED2 as wake up pin)