

## Data sheet 修改記錄單

Part No :	DM9003
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版 次	標準書修改記錄	日期	修改者
P01	1. New issue	113006	蔡長勳
P02	2. Add 10.2 Operating Conditions, PD (Power Dissipation). (P54). 3. Add 10.3 DC Electrical Characteristics, 100TX+/- Differential Output Current and 10TX+/- Differential Output Current, change to 19, 20, 21 mA, and 44, 50, 56 mA. (P54). 4. Add 11. APPLICATION CIRCUIT.(P58)	052307	蔡長勳
P03	1. 6. Vendor Control and Status Register Set, Product ID Registers change to 9003H, (P13) and 6.14 Product ID Registers ( 2AH~2BH ), (P17). 2. Add 6.19 TX/RX Memory Size Control Register ( 3FH ). (P18) 3. Add 6.41 Memory Data Read Command with Address Increment Register ( F2H ): RX memory size, defined in register 3FH with default 1F00H, and 6.42 Memory Data Read address Register ( F4H ): (RX memory size - 1), defined in register 3FH with default 1EFFH. (P29). 4. Add 7. EEPROM FORMAT: Word 29, Port 2 VLAN Tag. (P32) 5. Add 10.2 Operating Conditions, 1.8V / 3.3V of PD (Power Dissipation). (P54). 6. Add 10.4.1 Power On Reset Timing. (P55) 7. Add 13.Ordering Information: MAIL: <a href="mailto:sales@davicom.com.tw">sales@davicom.com.tw</a> and HTTP: <a href="http://www.davicom.com.tw">http://www.davicom.com.tw</a> (P60).	102207	蔡長勳
P04	1. Add 3.FEATURES, uP data driving capability adjustable, and Auto. Control to prevent memory read count error.(P10) 2. Add 6.CONTROL AND STATUS REGISTER SET, 0FH, 20H, 21H, 26H, 27H, 38H.(P15)	050908	蔡長勳

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	<ol style="list-style-type: none"> <li>3. Add 6.1 Bit 6, and 6.2 Bit5. (P17)</li> <li>4. Add 6.5 RX Status Register (06H): 3:2, Source Port Number.(P18)</li> <li>5. Add 6.11 Wake Up Control Register (0FH).(P19)</li> <li>6. Add 6.13 RX Packet Length Low Register ( 20H ), 6.14 RX Packet Length High Register ( 21H ), 6.15 RX Additional Status Register ( 26H ), 6.16 RX Additional Control Register ( 27H ), 6.22 uP Data Bus driving capability Register (38H). (P19 - 21)</li> <li>7. Modify 6.38 Per Port Priority Queue Control Register (6DH), Bit5, Description: Weighted Round-Robin Queuing.(P27)</li> <li>8. Add 7.EEPROM FORMAT, Word 7, Bit 13:12 reserved, set 00 in application. Word 16, Bit 15:12 = Reserved, set 0000 in application. Word 56, Set to 0 in application.(P33 – 35)</li> <li>9. Add 8.15 (Specified config) Register – 20H, and 8.16 Power Saving Control Register (PSCR) – 29H.(P46 – 48)</li> <li>10. Modify 9.2.14 Priority Support, The DM9003 provides two packet scheduling algorithms: Weighted Round-Robin Queuing.(P51)</li> <li>11. Modify 10.2 Operating Conditions, PD (Power Dissipation).(P57)</li> <li>12. Modify 10.4.2 Processor I/O Read Timing, System Data(SD) Delay time (T5) to 25 ns, and IOR# invalid to System Data(SD) invalid (T6) to 10 ns.(P60)</li> </ol>		