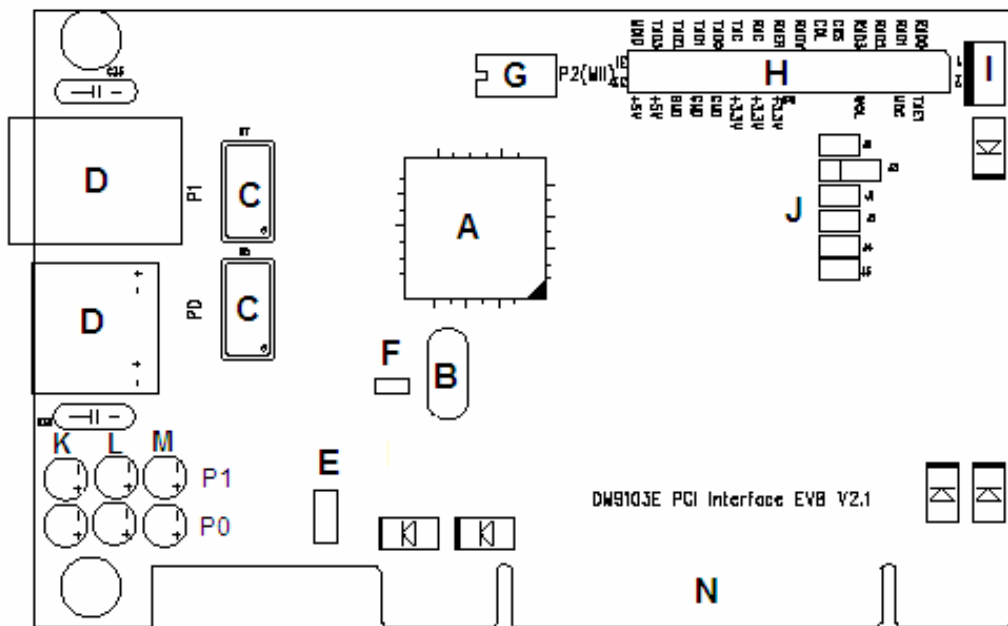


# DM9103 PCI Evaluation Board

## User Menu

The user menu for the DM9103 PCI evaluation board provides information for a design engineer to be able to connect the DM9103 to any architecture. The DM9103 PCI evaluation board is shown below.



A	DM9103	H	MII (P2) Interface Connector
B	25MHz Crystal	I	WOL Connector
C	P0 & P1 10/100M Transformer	J	Jumper Setting
D	P0 & P1 RJ-45 Phone Jack	K	P0 & P1 Link/ACT status LED
E	5V to 3.3V Regulator	L	P0 & P1 Speed status LED
F	3.3V to 1.8V Transistor	M	P0 & P1 FDX status LED
G	93LC46 EEPROM	N	PCI Interface Connector

The detailed description of the table above is shown respectively below.

### A. DM9103

The DM9103 is a fully integrated, high performance, and cost-effective fast Ethernet switch controller with one general PCI bus interface, two ports 10M/100Mbps PHY, and one port MII / Reverse MII or RMIi interface, and is designed for the embedded system applications. The AUTO-MDIX switching capability to fit straight through or crossover cables is also supported.

**B. 25MHz Crystal**

The requirement of the crystal is of 25MHz +/-30ppm.

**C. P0 & P1 10/100M Transformer**

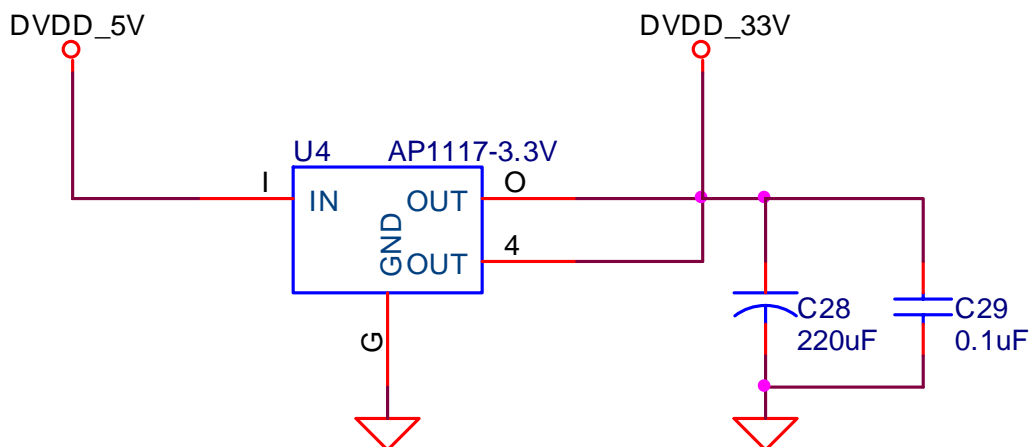
The suitable transformers shown as follows are for the design engineers' reference.

Vendor	Part Number
GTS	FC-621SM
YCL	PH163539
BOTHHAND	TS6121CX
MAGCOM	HS9016, HS9024

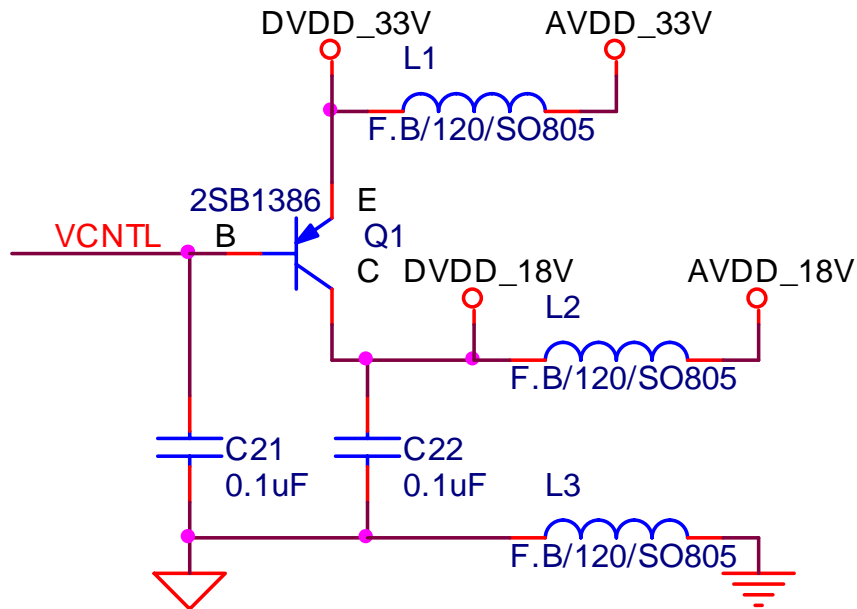
**D. P0 & P1 RJ-45 Phone Jack**

**E. 5V to 3.3V Regulator**

The reference circuit of 5V to 3.3V regulator is shown below. The type of regulator U4 is SOT-223. The design engineer should take notice of that the specification of the regulator chosen should be the same as the regulator U4 mentioned above and the output voltage should be fixed on 3.3V.

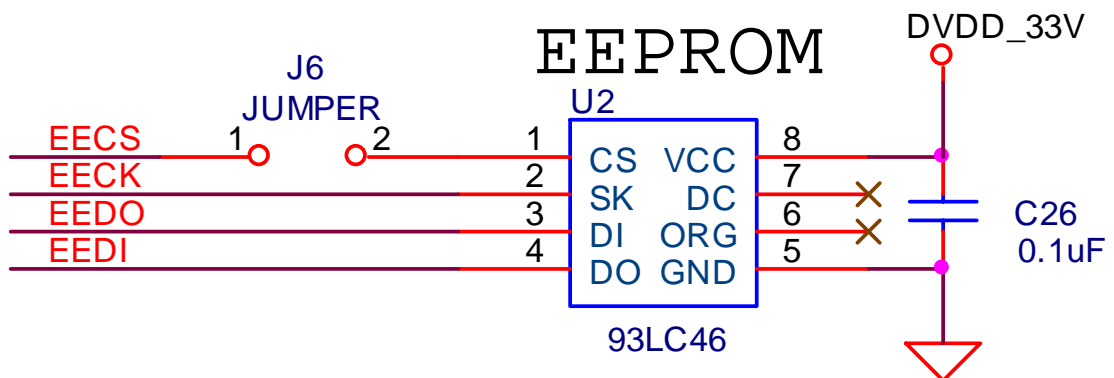


F. 3.3V to 1.8V Transistor

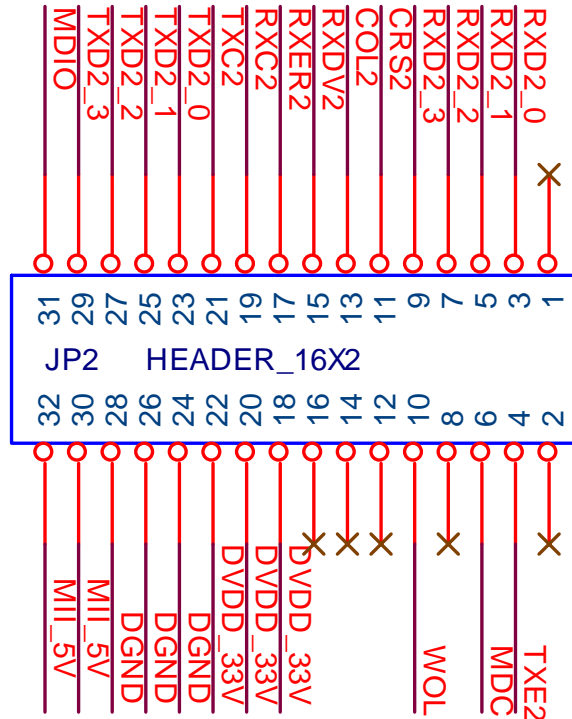


G. 93LC46 EEPROM

The package of 93LC46 is DIP8. In addition, the specification of the 93LC46 should be the same as the figure below.



H. MII (P2) Interface Connector



I. WOL Connector (JP1)

Pin1: +5V

Pin2: Ground

Pin3: WOL signal

J. Jumper setting:

1. J1:

The port1 / port2 disable select. (for 2 port mode only).

OFF: port 2 disabled

ON: port 1 disabled

2. J2:

The P2 / P1 Disable (for 2 port mode only).

OFF: Port 2 status from external PHY

ON: Port 2 status in force mode

3. J3:

2 port / 3 port select

Pin 1- 2 on: 3 port mode

All ports are active in this mode.

Pin 2-3 on: 2 port mode

Only 2 ports are active in this mode. Port 1 or port 2 can be disabled by strap TXEN2. In this mode, the memory resource is shared by PCI bus port and the other 2 ports.

4. J4, J5

The P2 MII / RMII / Reverse-MII force link mode.

J4	J5	
0	0	Port 2 is MII mode (Default)
0	1	Port 2 is in reverse MII mode
1	0	Port 2 is in RMII mode and memory BIST disabled
1	1	Port 2 is in RMII mode

5. J6

The EEPROM select

On: Enable EEPROM 93C46

OFF: Disable EEPROM 93C46

K. P0 & P1 Link/ACT status LED

The LINK/ACT LED is the link LED. If the LINK/ACT LED is on, it represents the link status is good. If the LINK/ACT LED is blinking, it presents that data are transmitting or receiving. If the LINK/ACT LED is off, it is probably that the link status is off or failure.

L. P0 & P1 Speed Status LEDs

The SPEED LED represents the link speed is 10M or 100Mbps.

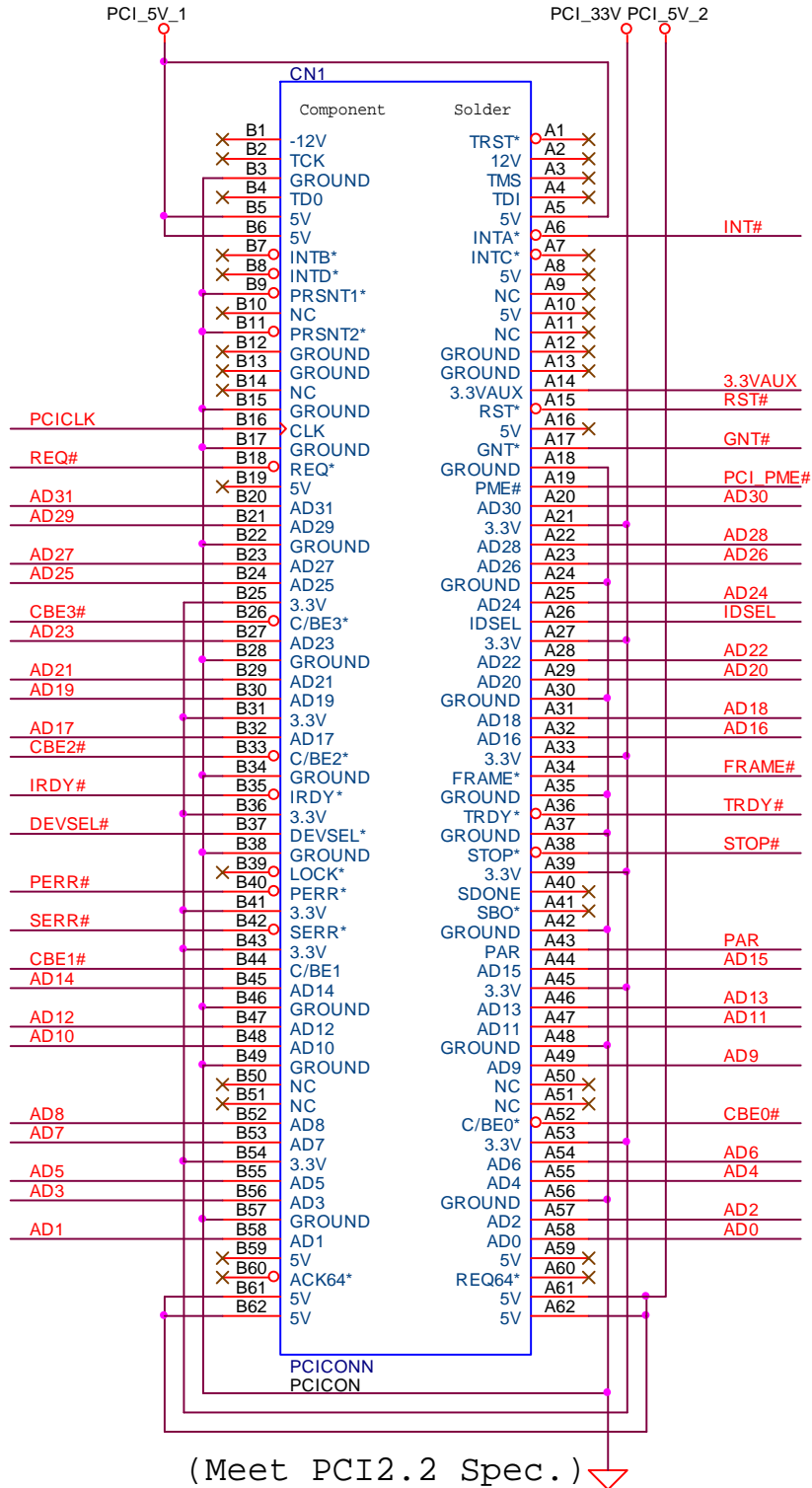
If the SPEED LED is on, the link speed is 100Mbps. If the SPEED LED is off, the link speed is 10Mbps or link fails (depend on the LINK/ACT LED).

M. P0 & P1 FDX status LED

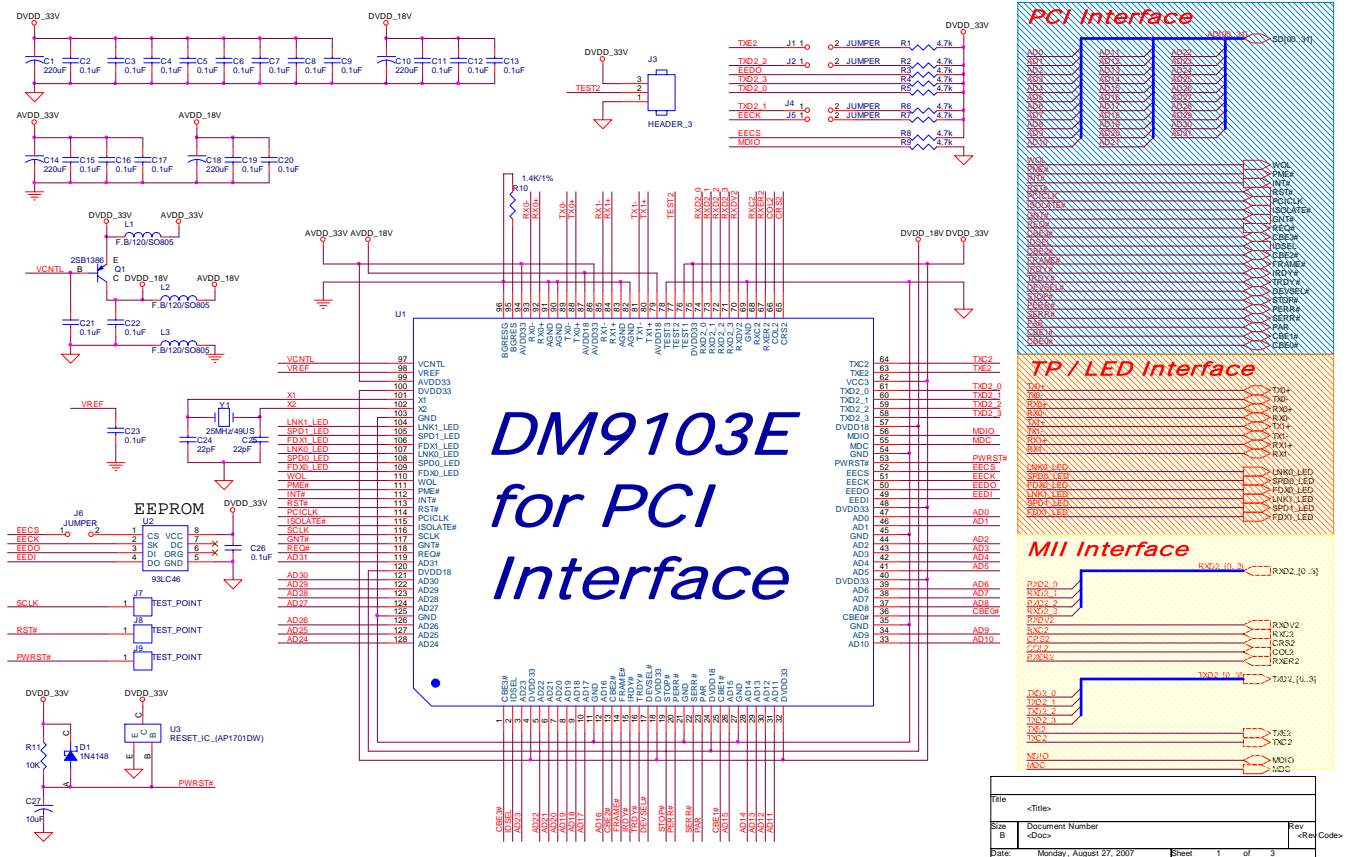
The FDX LED represents the Full Duplex status,

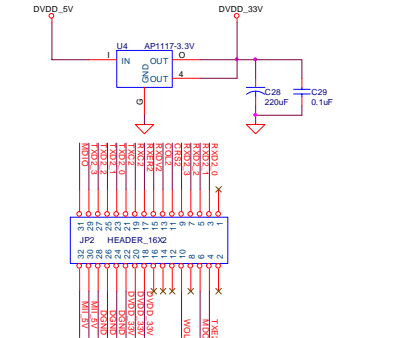
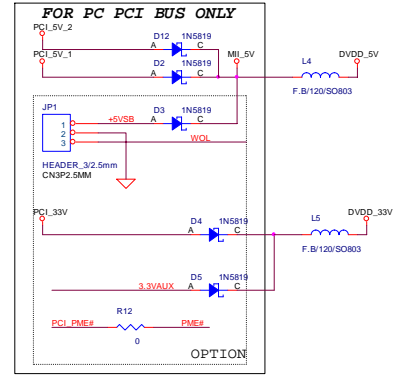
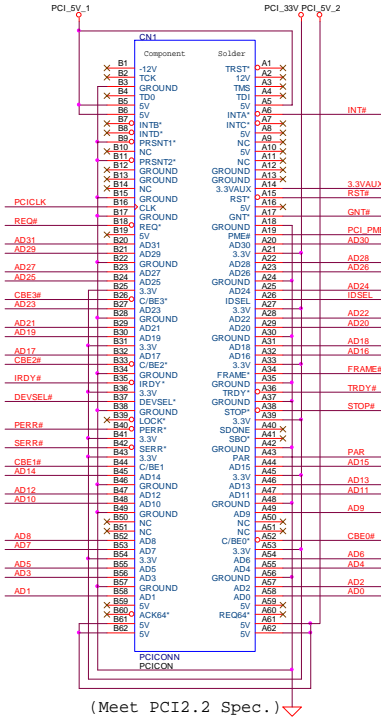
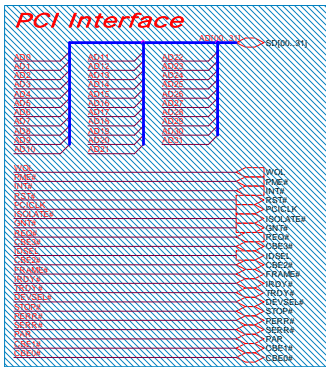
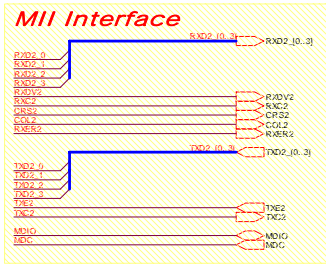
If the FDX LED is on, the status is Full Duplex. If the FDX is off, the Status is Half Duplex.

## N. PCI Interface Connector

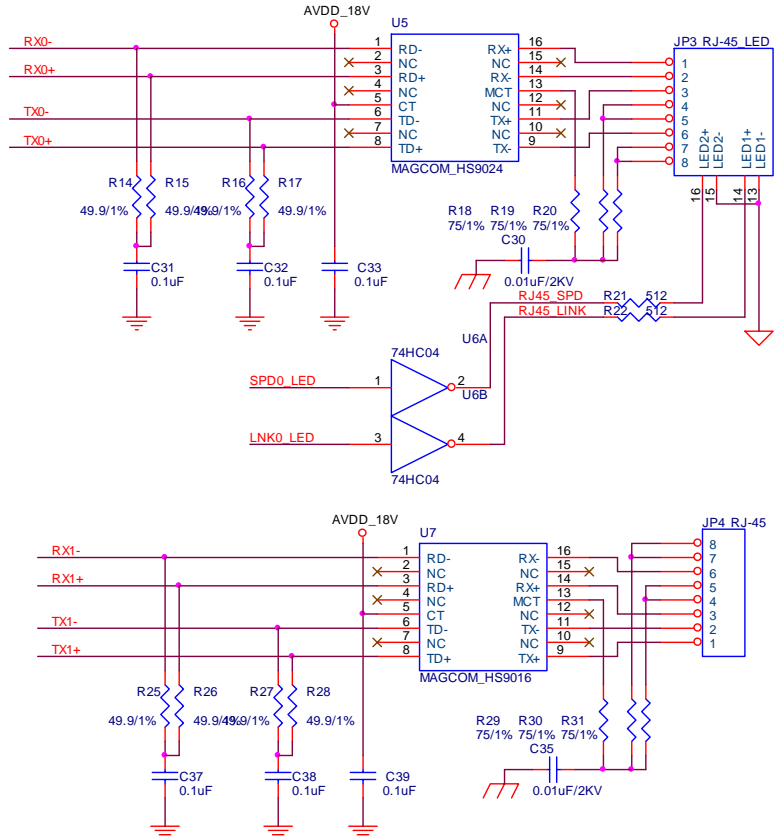
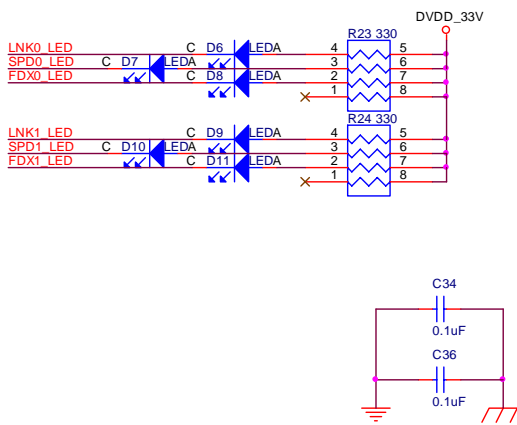
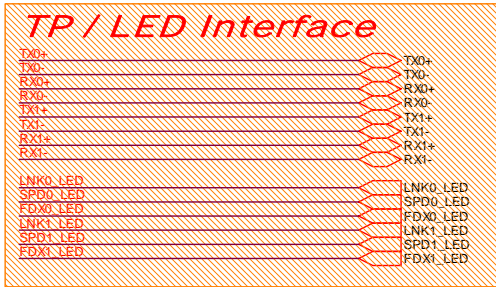


Reference circuit:





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Code	<Code>



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