



DM9161A / DM9161E

Power on reset

Application Notes

DM9161A / DM9161E

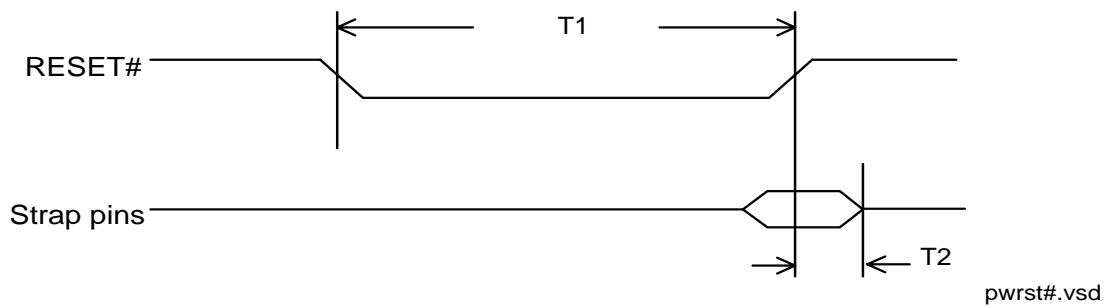
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Application Notes

Davicom Semiconductor, Inc

1. Power On Reset:

An active low signal is used to reset the DM9161A / DM9161E chip. The RESET# pin 40 is asserted low for at least 10 ms. All of the PHY registers will be reset to the default values and the hardware strap pins will also be latched.

2. Power On Reset Timing:


Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition s
T1	RESET# Low Period	10	-	-	ms	-
T2	Strap pin hold time with RESET#	40	-	-	ns	-

2. Power On Reset application circuit:

