

DM9161A – Additional datasheet information

Please note that DM9161AE pin 1, 2, 9 are AVDD 2.5V power output. You cannot connect AVDDR1, 2 and AVDDT (2.5V) to +3.3V. If you want set DM9161AE in auto-negotiation mode, please pull up pin 11, 12, and 13. Or, you can set DM9161AE in other mode. For detail information, you can refer to DM9161AE datasheet table 5.7 about op mode setting.

To prevent noise, please used ferrite bead, 120Ohm between AVDD_TX and AVDD_RX become AVCC (2.5V internal regulator out-put pin 1, 2, 9), this voltage used as reference connected to master CT of MDIX type Magnetic (Taimag HA-103). For None MDIX along with pin 39 must pulled-high, the 2.5V AVCC must connected to CT tap of TX and RX portion of Magnetic.

The C11, C27 value and type certification of capacitor can be changed via designer experiment through hardware lay-out. Electrolytic or Ceramic would be fine.

The pin 5 (RJ45 RX choke) has to connect to 2.5V as well. If you pull up pin 39, you set the auto-mdix function to disabled.

Please pull up LED0 and RXCLK pin by two 1K ohm resistors to make sure that they were pulled up correctly.

If you use an crystal as a 25MHz timing source, the XT1 pin 43 is crystal timing input pin. But if you use an oscillator or other timing source, the XT2 pin 42 is clock timing input pin. For RMII mode, the XT2 pin 42 will be the 50MHz clock timing input. And the pin 36 COL/RMII will be pulled up to make the RMII mode enable.

If bit3 of register 17 is 1 means auto-negotiation complete successfully.

ISOLATE and PHYAD [0..4] have internal pull down 60k. The AVDDT and AVDDR can be connected tighter.