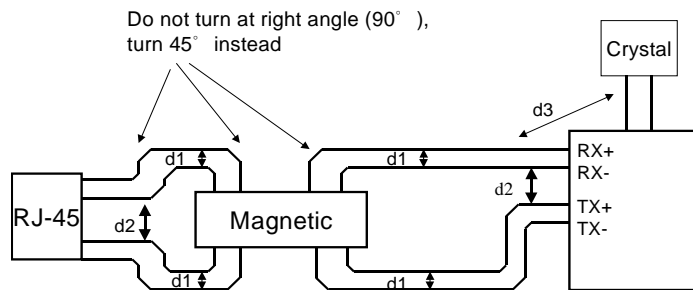


1. Placement, Signal and Trace Routing

- Place the 10/100M magnetic as close as possible to the DM9161A (no more than 20mm) and to the RJ-45 connector.
- Place the termination resistors 50Ω as close as possible to the 10/100M magnetic and the DM9161A RX \pm pins and TX \pm pins. The 50Ω resistors and grounding capacitors of TX \pm and RX \pm should be placed near DM9161 (no more than 10mm).
- The 25MHz crystal should not be placed near important signal traces, such as RX \pm receive pair and TX \pm transmit pair, band gap resistor, magnetic and board edge.
- Traces routed from the DM9161A RX \pm pair to the 10/100M magnetic and the RJ45 connector should run symmetrically, directly, identically, and closely (no more than 2mm). The same rule is applied to traces routed from the DM9161A TX \pm pair.

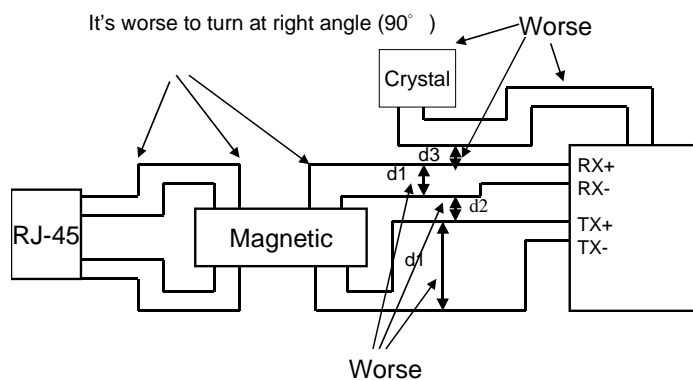


better

$d1 < 2\text{mm}$

$d2 > 3\text{mm}$; having AGND as a shield is better

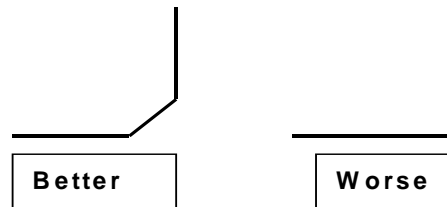
$d3 > 5\text{mm}$; having AGND as a shield is better



DM9161A Layout Guide



- It is recommended that RX±receive and TX±transmit traces turn at 45° angle. Do not turn at right angle.



- Avoid using vias in routing the traces of RX± pair and TX± pair.
- The RX±pair, TX±pair, clock, and power traces should be as short and wide as possible.
- Do not place the DM9161A RX±receive pair across the TX±transmit pair. Keep the receive pair away from the transmit pair (no less than 3mm). It's better to place ground plane between these two pairs of traces.
- The network interface (see Figure 3-1 and Figure 4) does not route any digital signal between the DM9161A RX±and TX±pairs to the RJ-45. Keep the two pairs away from all the other active signals and the chassis ground.
- It should be no power or ground plane in the area under the network side of the 10/100M magnetic and the area under the RJ-45 connector.
- Any terminated pins of the RJ-45 connector (pins 4,5,7 and 8, see Figure 1) and the magnetic (see Figure 1) should be tied as closely as possible to the chassis ground through a resistor divider network 75Ω resistors (no more than 2mm to the magnetic) and a 0.01μF/2KV bypass capacitor.
- The Band Gap resistor should be placed as close as possible to pins 47 and 48 (BGRES, BGRESG) (no more than 3mm). Avoid running any high-speed signal near the Band Gap resistor placement (no less than 3mm from 25MHz XT1 and XT2).

DM9161A Layout Guide



10Base-T/100Base-TX Application

Figure 1-1 and 1-2 illustrate the two types of the specific magnetics interconnect and how to connect with Davicom DM9161A. These magnetics are not pin-to-pin compatible. Please must be considered when using the DM9161A in auto-MDIX mode.

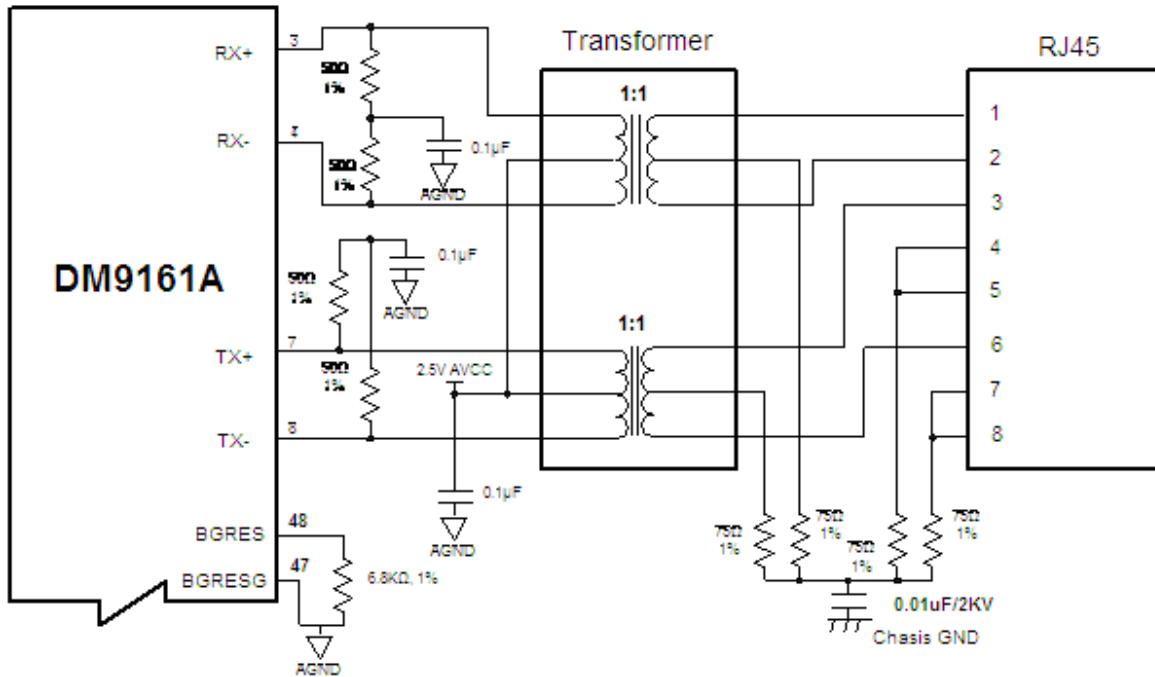


Figure 1-1

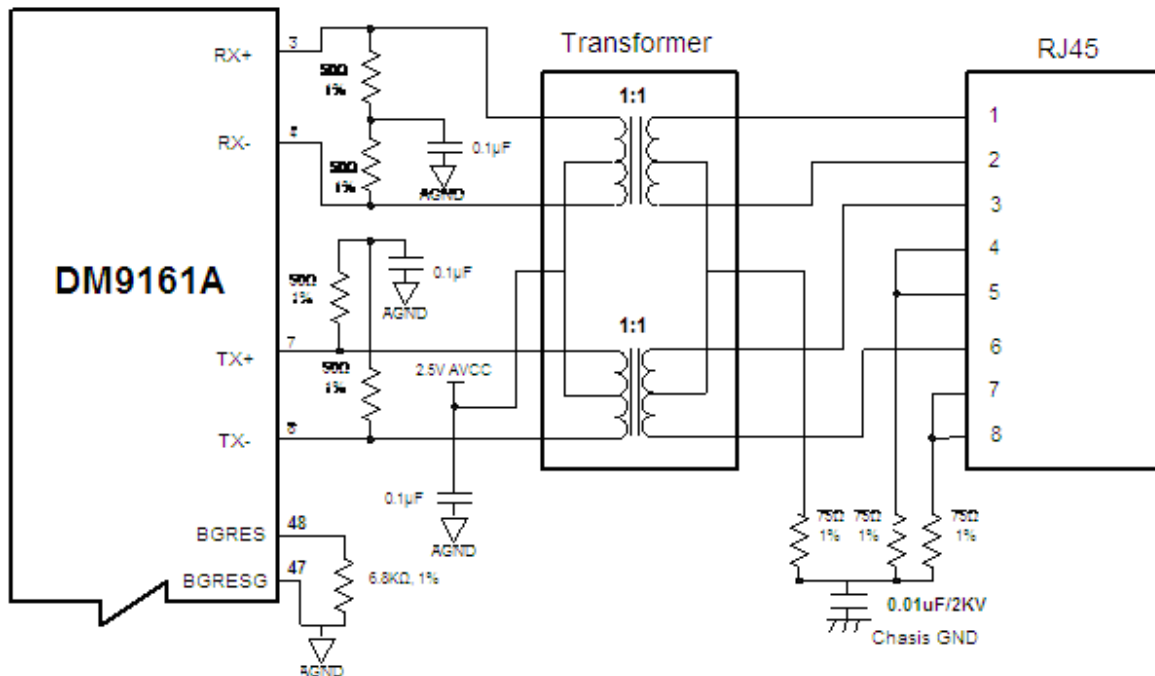


Figure 1-2

2. Power Supply Decoupling Capacitors

- Place all the decoupling capacitors for all power supply pins as close as possible to the power pads of the DM9161A (no more than 2.5mm from the above mentioned pins). The recommended decoupling capacitor is 0.1 μ F or 0.01 μ F.
- The 0.1-0.01 μ F decoupling capacitor should be connected between each DVDD/DGND set and AVDD/AGND set and be placed as close as possible to the pins of DM9161A. The conservative approach is to use two decoupling capacitors on each DVDD/DGND set and AVDD/AGND set. One 0.1 μ F is for low frequency noise, and the other 0.01 μ F is for high frequency noise on the power supply.
- The AVDD connection to the transmit center tap of the magnetic has to be well decoupled to minimize common mode noise injection from the power supply into the twisted pair cable. It is recommended that a 0.01 μ F decoupling capacitor should be placed between the center tap AVDD to AGND ground plane. This decoupling capacitor should be placed as close as possible to the center tap of the magnetic. 100 μ F capacitor should be connected between each AVDD and AGND. 100 μ F capacitor should be connected between each AVDD and AGND.

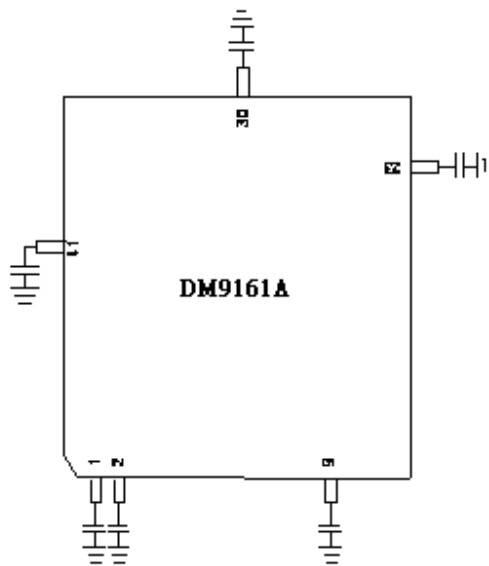


Figure 2

3. Ground Plane Layout

- Place a single ground plane approach to minimize EMI. Ground plane partitioning can cause increased EMI emissions that could make the network interface card (NIC) not comply with specific FCC part 15 and CE regulations.
- Ground plane need separate analog ground domain and digital ground domain, the analog ground domain and digital ground domain connected line is far away the AGND pins of DM9161A (see Figure 4-1).
- All AGND pins (pin 5, 6, 46) could not directly short each other (see Figure 3-3). It must be directly connected to analog ground domain (see Figure 3-2).
- Analog ground domain area is as large as possible

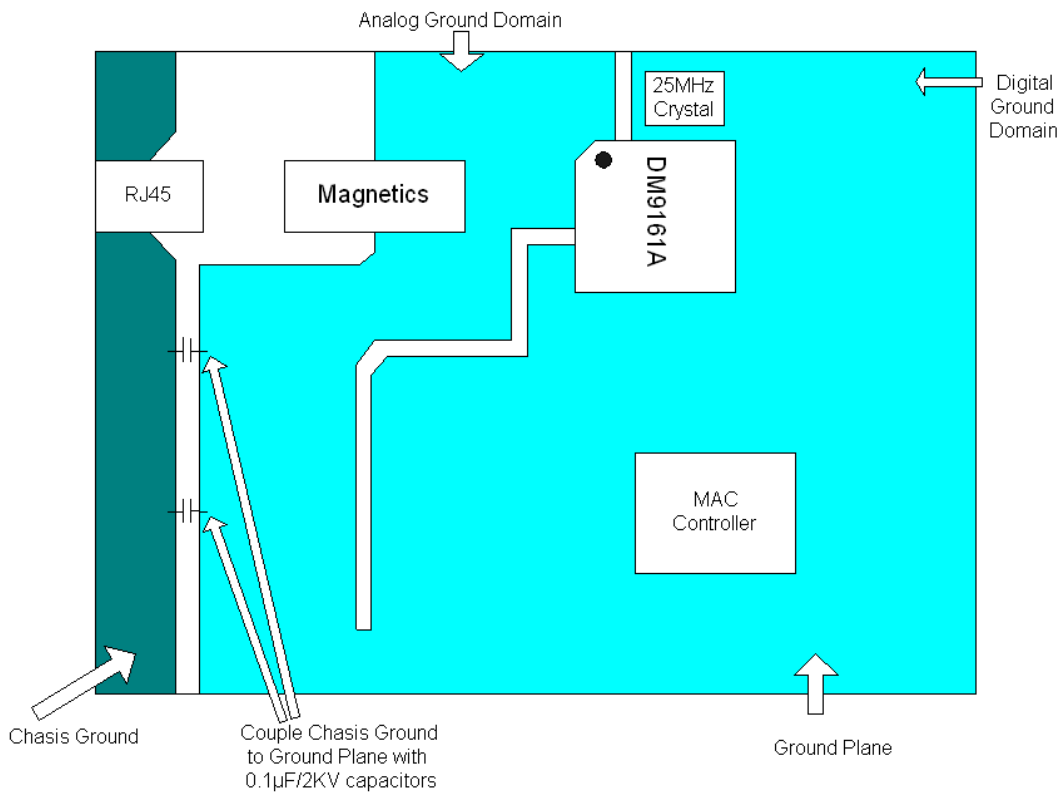


Figure 3-1

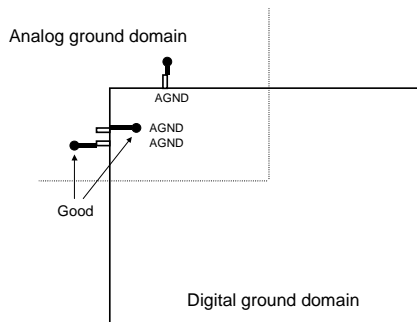


Figure 3-2

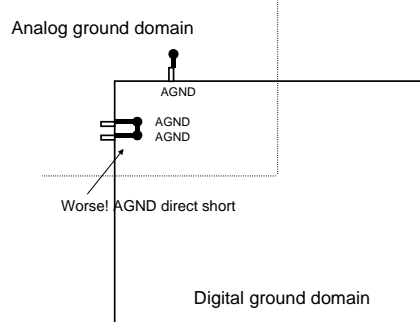


Figure 3-3

4. Power Plane Partitioning

- The power planes should be approximately illustrated in Figure 4.

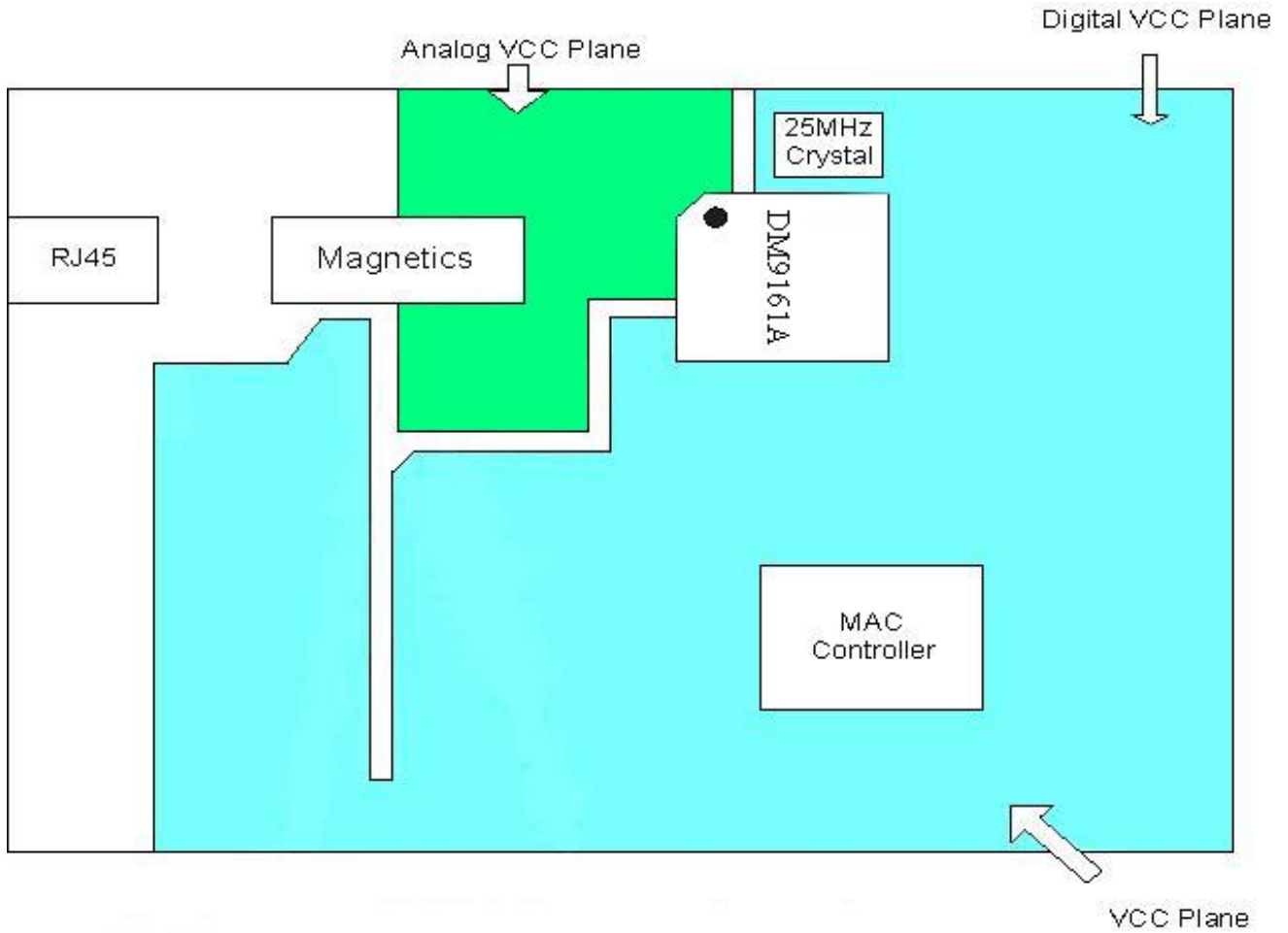


Figure 4

5. Magnetics Selection Guide

- Refer to the following tables 5-1 and 5-2 for 10/100M magnetic sources and specification requirements. The magnetics which meet these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetic specifications before using them in an application. The magnetics listed in the following table are electrical equivalents, but may not be pin-to-pin equivalents.

Manufacturer	Part Number
Pulse Engineering	PE-68515, H1102
YCL	PH163112, PH163539
Halo	TG110-S050N2, TG110-LC50N2
Bel Fuse	S558-5999-W2
Bothhand	TS6121CX, LU1S041CX TS6121C, 16ST8515, 16ST1086
GTS	FC-618SM

Table 5-1: 10/100M Magnetic Sources

Parameter	Values	Units	Test Condition
Tx / RX turns ratio	1:1 CT / 1:1	-	-
Inductance	350	μH (Min)	-
Insertion loss	1.1	dB (Max)	1 – 100 MHz
Return loss	-18	dB (Min)	1 – 30 MHz
	-14	dB (Min)	30 – 60 MHz
	-12	dB (Min)	60 – 80 MHz
Differential to common mode rejection	-40	dB (Min)	1 – 60 MHz
	-30	dB (Min)	60 – 100 MHz
Transformer isolation	1500	V	-

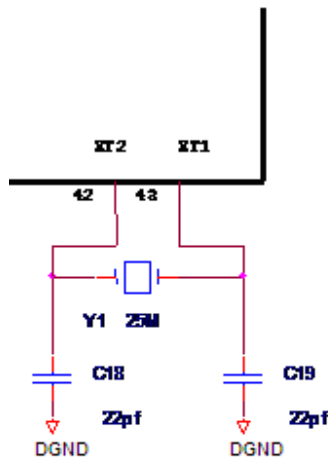
Table 5-2: Magnetic Specification Requirements

6. Crystal Selection Guide

- A crystal can be used to generate the 25MHz reference clock instead of an oscillator. The crystal must be a fundamental type, parallel resonance, connect to XT1 and XT2, and shunt each crystal lead to ground with a 22pF capacitor as shown in Figure 6.

PARAMETER	SPEC
Type	Fundamental, parallel resonance
Frequency	25 MHz +/- 0.01%
Equivalent Series Resistance	25 ohms max
Load Capacitance	22 pF typ.
Case Capacitance	7 pF max.
Power Dissipation	1mW max.

Table 6-1: Crystal Specifications



**Figure 6
Crystal Circuit Diagram**

7. MII Signals to MAC Controller

- The length of the trace routing for the Media Independent Interface (MII) signals should be as short and direct as possible between the DM9161A and MAC controller (Maximum shorter than 20cm). These MII signals are as follows,

CRS, COL, TXD3, TXD2, TXD1, TXD0, TXEN, TXCLK, TXER
RXER, RXCLK, RXDV, RXD0, RXD1, RXD2, RXD3, MDC, MDIO

- TXD[0-3] and TXCLK length mismatch does not exceed 2cm.
- RXD[0-3] and RXCLK length mismatch does not exceed 2cm.