

UZ2400

Silicon Version D

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

U-Power500D Module AN-2400-63

Version: 0.0

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UZ2400

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

1. General Information

The U-Power500D module is an IEEE 802.15.4 compliant solution that satisfies the requirements of low-power and long-range wireless applications. The module contains UBEC's UZ2400 Silicon Version D, UP2268 and other necessary components operating in the ISM 2.4 GHz frequency band. The corresponding MCU can access various UZ2400 internal subunits, such as registers, FIFOs, and security key table, via a 4-wire SPI bus. Its small form factor saves the valuable board spaces and provides a reliable delivery of critical data between the devices.

2. Features

- 2.4GHz IEEE 802.15.4 compliant
- 3.0 ~ 3.6V Operation
- Sleep current: 3 μ A, typical
- Effective distance: 500 meters (line of sight , environment dependent, typical)
- PCB antenna
- Additional GSG (ground-signal-ground) interfaces provided
- RX sensitivity: -101dBm, typical
- TX output Power: 11dBm, typical
- TX current consumption: 40mA, typical
- RX current consumption: 29mA, typical
- Dimension: 48.3mm x 14mm x 2.3mm

3. Pin Configuration

3.1. Pin Assignment

Top view of a U-Power500D module and pin allocation map are shown in Figure 1 and Figure 2 respectively

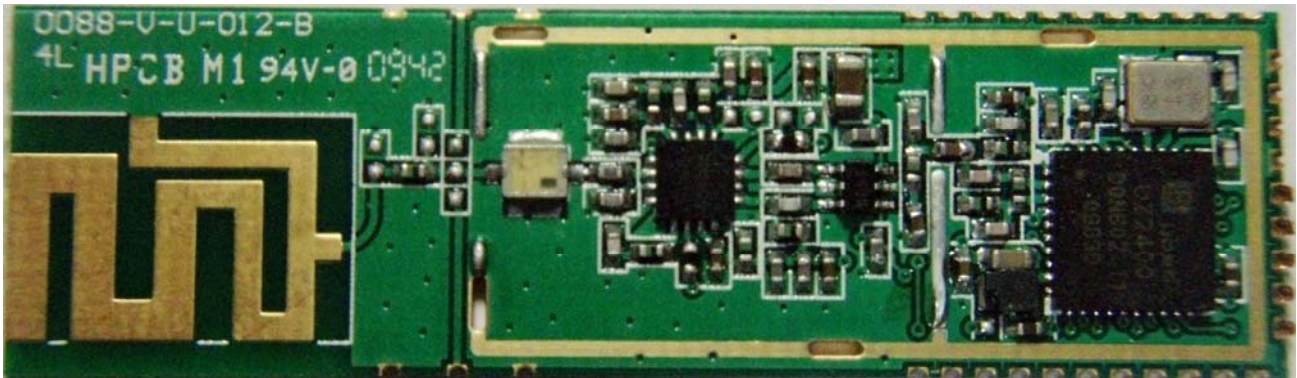


Figure 1. Top View of U-Power500D Module

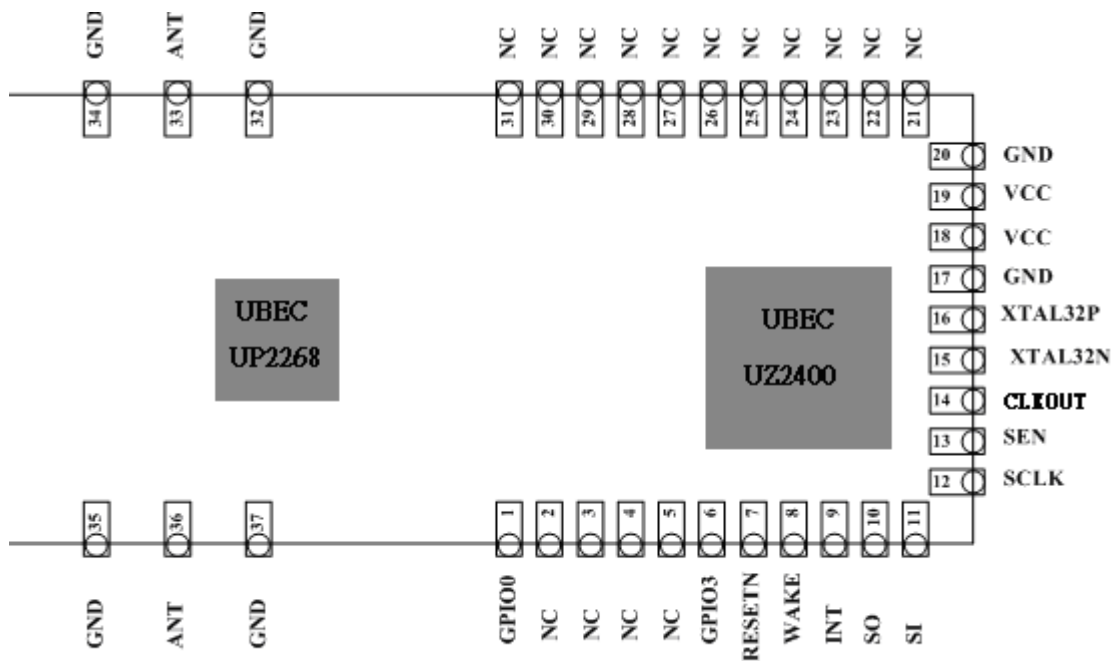


Figure 2. Pin Allocation

3.2. Pin Description

Pin type abbreviation: A = Analog, D = Digital, I = Input, O = Output, P = Power, G = Ground

Pin	Name	Type	Description
1	GPIO0	DIO	General purpose digital I/O, also used as an external PA enable
2	NC		No Connection
3	NC		No Connection
4	NC		No Connection
5	NC		No Connection
6	GPIO3	DIO	General purpose digital I/O
7	RESETN	DI	Global hardware reset pin, active low
8	WAKE	DI	External wake up trigger, active high / low can be programmable.
9	INT	DO	Interrupt pin to micro-processor : Level trigger, Hi / Low programmable
10	SO	DO	Serial interface data output from UZ2400 or I2C clock
11	SI	DI	Serial interface data input to UZ2400 or I2C data in/out
12	SCLK	DI	Serial interface clock
13	SEN	DI	Serial interface enable
14	CLKOUT	DO	32 / 16 / 8 / 4 / 2 / 1 MHz clock output
15	XTAL32N	AI	32 kHz Crystal input (-) for internal RTC used
16	XTAL32P	AI	32 kHz Crystal input (+) for internal RTC used
17	GND	G	Ground
18	VCC	PI	Power Supply
19	VCC	PI	Power Supply
20	GND	G	Ground
21-31	NC		No Connection
32	GND	G	Ground
33	ANT	RF	Antenna Port
34	GND	G	Ground
35	GND	G	Ground
36	ANT	RF	Antenna Port
37	GND	G	Ground

Table 1. Pin Assignment

4. Electrical Specifications

Test conditions: $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$

ITEM	Condition	Specification			Unit
		Min.	Typ.	Max.	
Frequency		2405		2480	MHz
Supply voltage		3	3.3	3.6	V
TX Current consumption	$P_{out}=11\text{dBm}$		40		mA
RX Current consumption			29		mA
TX Output power	$P_{out}(\text{UZ2400})=0\text{dBm}$		11		dBm
TX EVM	$P_{out}(\text{UZ2400})=0\text{dBm}$		18		%
RX sensitivity	PER \leq 1% O-QPSk 250kbps		-101		dBm
Communication Range	Throughput >120kbps at 250kbps data rate, LOS		500		m

Table 2. Electrical Specifications

For detail electrical characteristic of the UZ2400 chip, please refer to UZ2400 datasheet (DS-2400-51).

4.1. TX Output Power

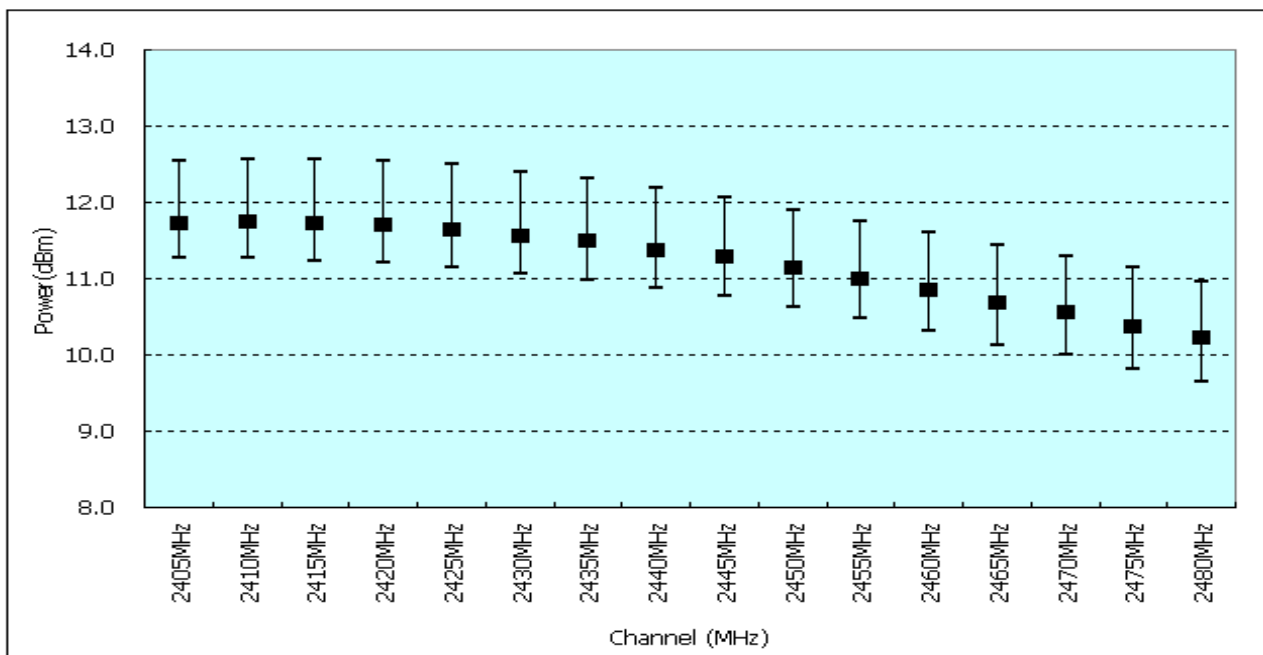


Figure 3. Typical TX Output Power

4.2. TX EVM

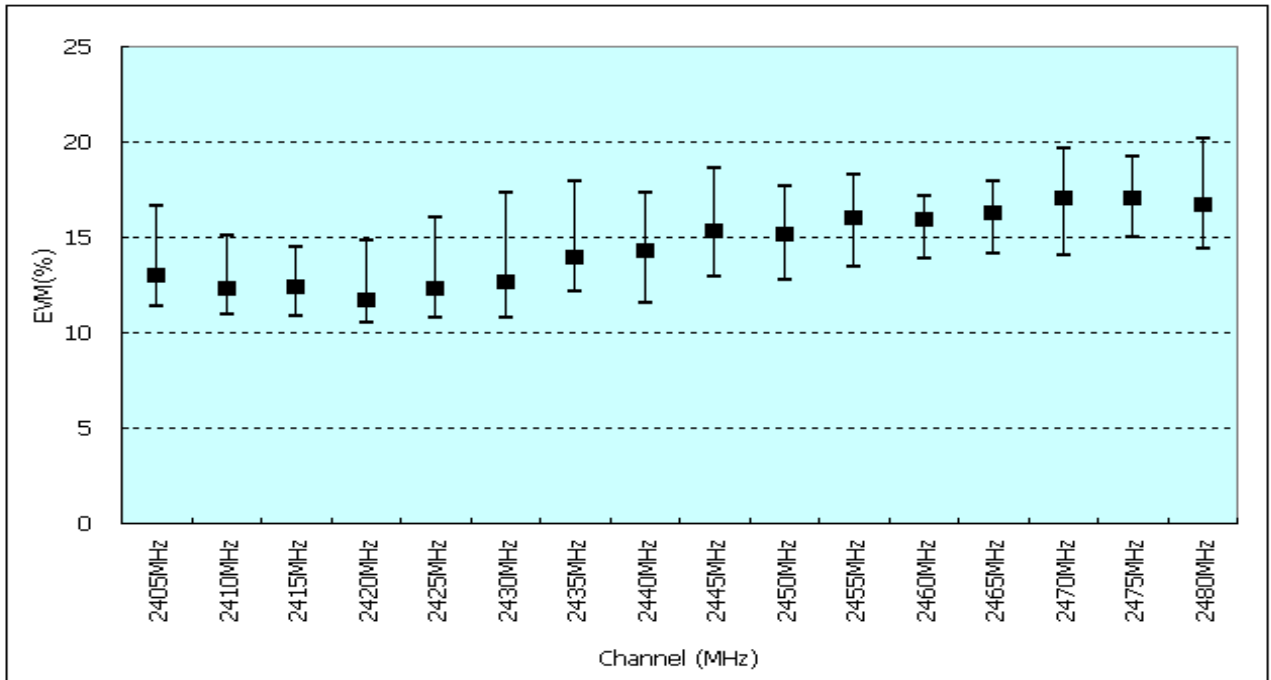


Figure 4. Typical TX EVM (P_{out} shown in Figure 3)

4.3. RX Sensitivity

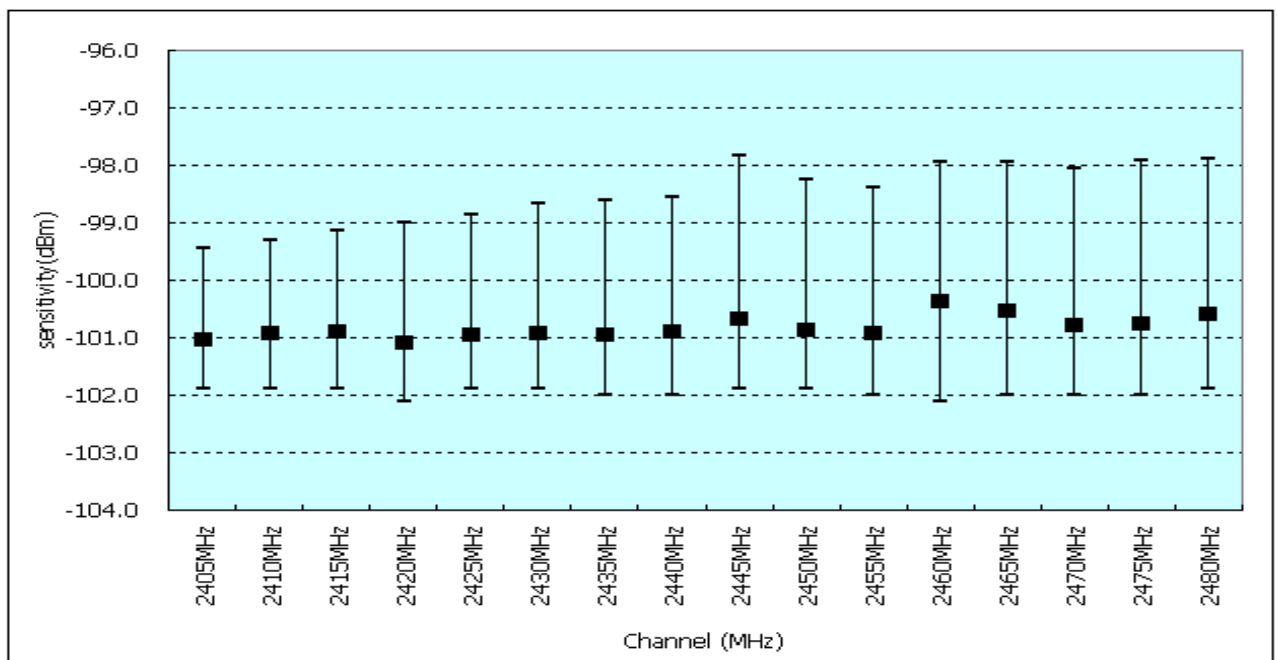


Figure 5. Typical RX Sensitivity

5. Register Initial Setting

The procedure to configure the module is described as below.

Step 1. Initialization

Refer to UZ2400 datasheet (DS-2400-51) section 4.3.1 to initialize this module

Step 2. Set Channel

Refer to UZ2400 datasheet (DS-2400-51) section 4.3.

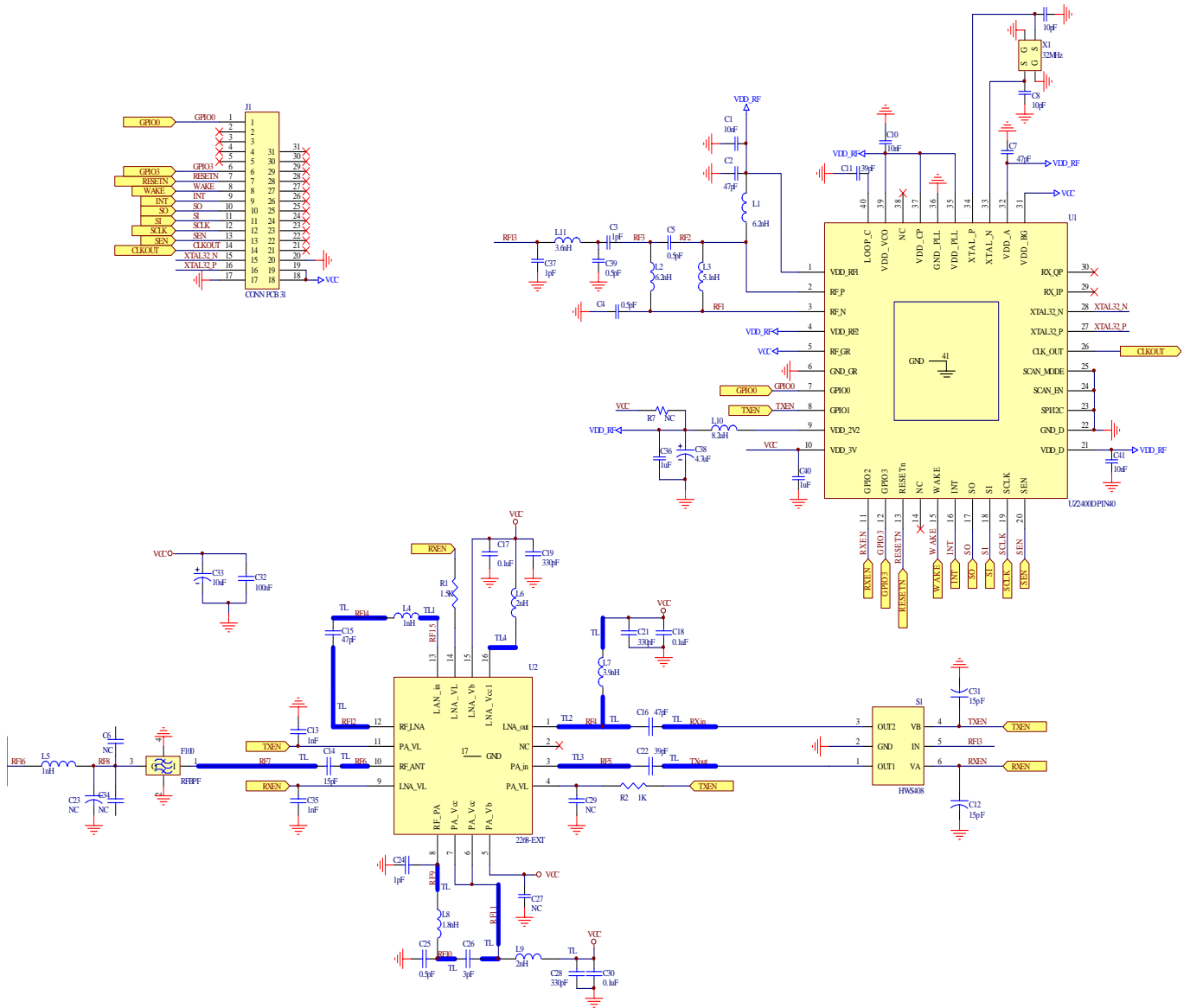
Step 3. RESET

Refer to UZ2400 datasheet (DS-2400-51) section 4.3.

Step 4. PA/LNA Control

Address mode	Address	Register Name	Descriptions	Setting Value(hex)
LREG	0x22F	TESTMODE	GPIO0, GPIO1, GPIO2 are configured to control external PA, LNA or switch	0x29
LREG	0x203	RFCTL3	RF maximum output power setting (Refer to UZ2400 datasheet Appendix B. for different output power settings)	0x00

6. Schematic



7. PCB Layout

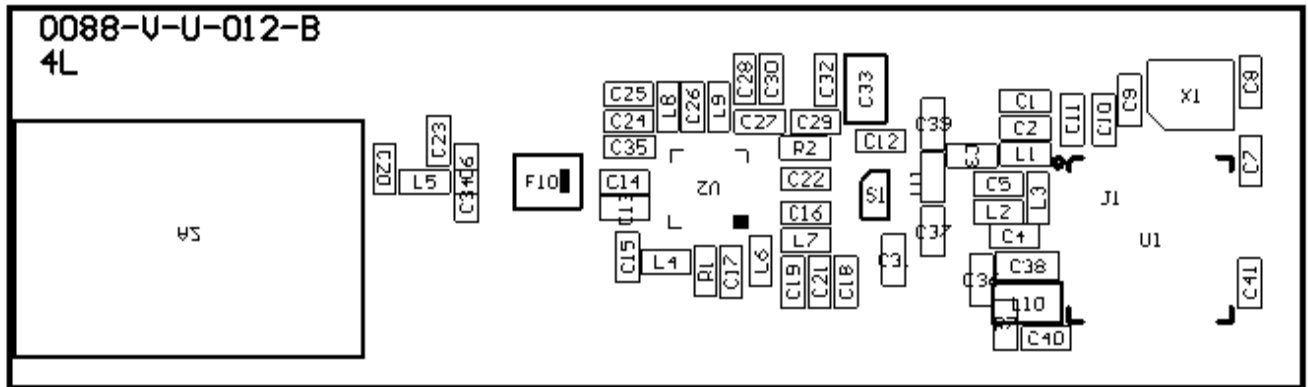


Figure 7. Top Overlay

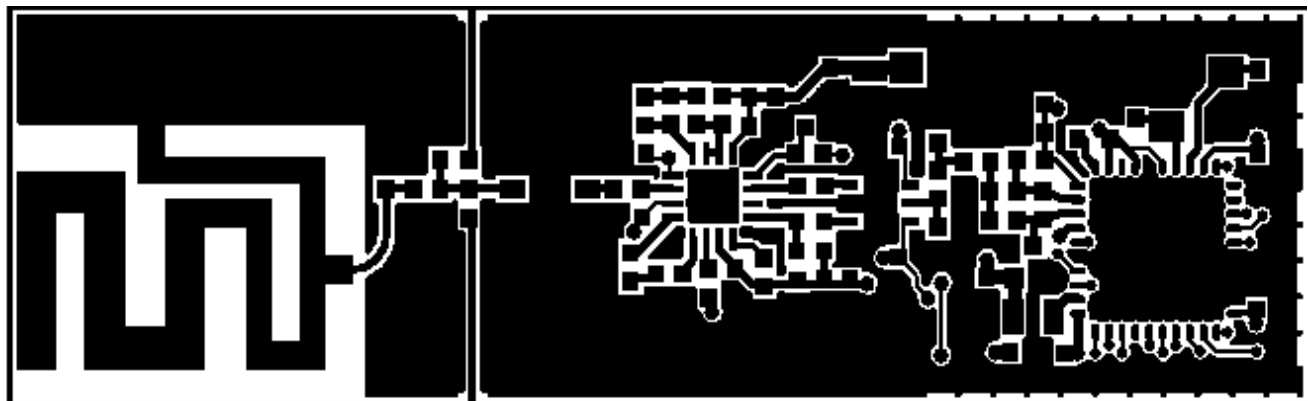


Figure 8. Top Layer (Signals)

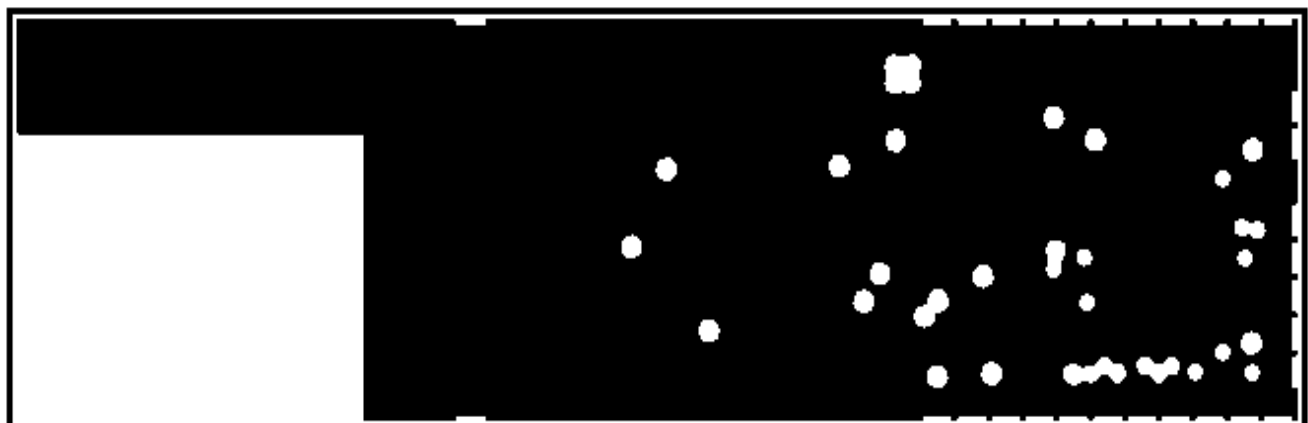


Figure 9. Midlayer2 (GND)

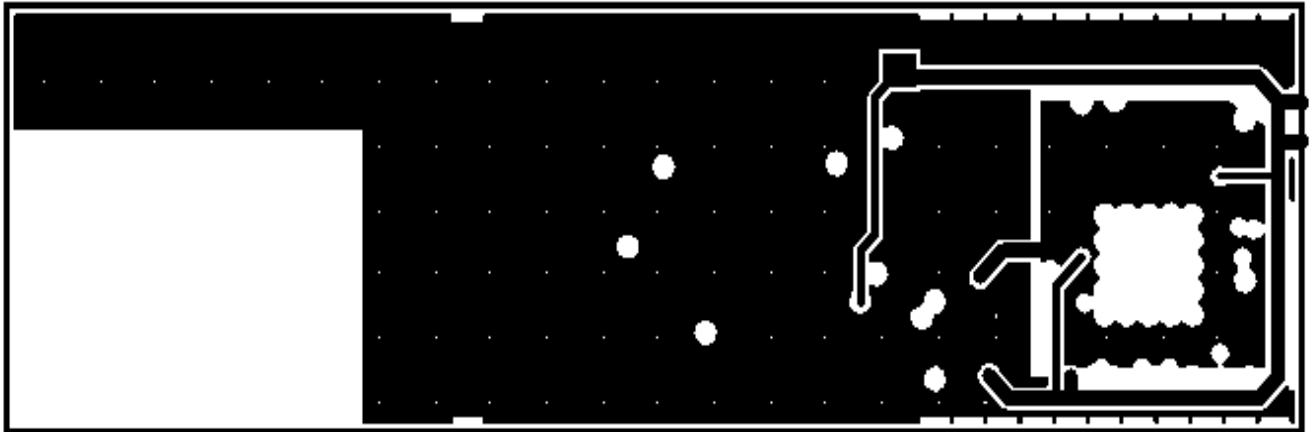


Figure 10. Midlayer3 (Power)

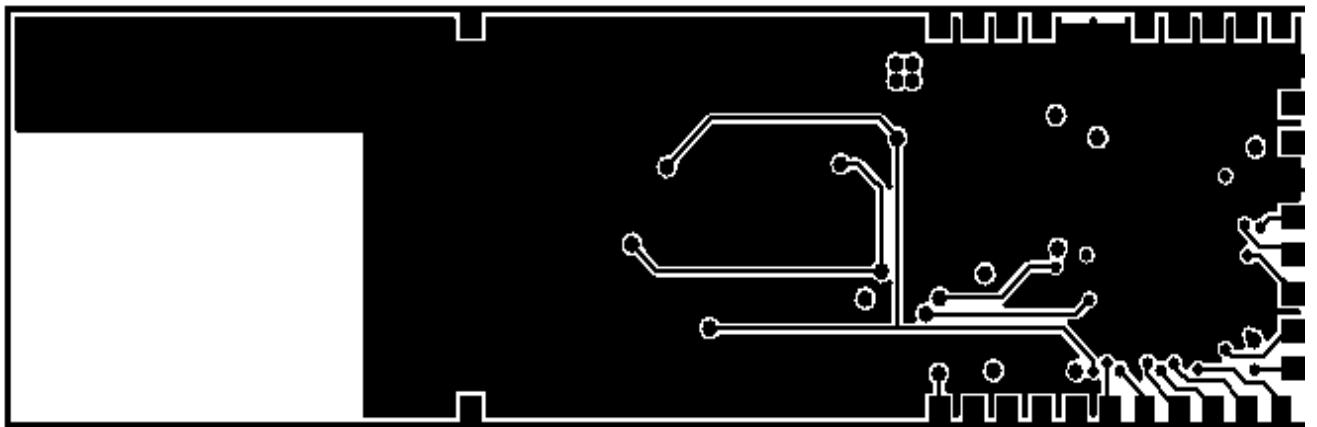


Figure 11. Bottom Layer (Signals and GND)

8. BOM List

Item	Part name	Footprint	Tolerance	Manufacturer	Vendor Part No	Qty	Reference
1	100nF	0402	16V Y5V -20~+80%	國巨	CC0402ZRY5V7BB104	4	C17
2	0.5pF	0402	50V NPO ±0.25pF	國巨	CC0402CRNPO9BNR50	4	C4
3	3.6nH	0402	±0.3nH	台灣村田	LQG15HN3N6S02	1	L11
4	1pF	0402	50V NPO ±0.25pF	國巨	CC0402CRNPO9BN1R0	3	C3
5	1.5K	0402	1/16W ±5%	國巨	RC0402JR-071K5L	1	R1
6	1K	0402	1/16W ±5%	國巨	RC0402JR-071K	1	R2
7	1nH	0402	±0.3nH	台灣村田	LQG15HN1N0S02	2	L4
8	1nF	0402	50V X7R ±10%	國巨	CC0402KRX7R9BB102	2	C13
9	1uF	0402	6.3V Y5V -20~+80%	國巨	CC0402ZRY5V5BB105	2	C36
10	1.8nH	0402	±0.3nH	台灣村田	LQG15HN1N8S02	1	L8
11	2nH	0402	±0.3nH	台灣村田	LQG15HN2N0S02	2	L6
12	3.9nH	0402	±0.3nH	台灣村田	LQG15HN3N9S02	1	L7
13	3pF	0402	50V NPO ±0.25pF	國巨	CC0402CRNPO9BN3R0	1	C26
14	5.1nH	0402	±0.3nH	台灣村田	LQG15HN5N1S02	1	L3
15	8.2uH	0806	±20%	台灣村田	LQH2MCN8R2M02	1	L10
16	4.7uF	0603	10V X5R ±10%	台灣村田	GRM188R61A475K	1	C38
17	10nF	0402	16V Y5V -20~+80%	國巨	CC0402ZRY5V7BB103	3	C1
18	10pF	0402	50V NPO ±5%	國巨	CC0402JRNPO9BN100	2	C8
19	10uF	0805	10V Y5V -20~+80%	國巨	CC0805ZKY5V6BB106	1	C33
20	6.2nH	0402	±0.1nH	台灣村田	LQP15MN6N2B02	2	L1
21	15pF	0402	50V COG ±5%	國巨	CC0402JRNPO9BN150	3	C12
22	CRYSTAL32MHz	CX_101F	15ppm/8pF/3.2*2.5mm	NDK	N3225SA	1	X1
23	39pF	0402	50V NPO ±5%	國巨	CC0402JRNPO9BN390	2	C11
24	47pF	0402	50V NPO ±5%	國巨	CC0402JRNPO9BN470	4	C2
25	330pF	0402	50V COG ±5%	國巨	CC0402KRX7R9BB331	3	C19
26	SWITCH /HWS408	SOT-363	GaAs/DC-2.5GHz/SPDT/SOT-363	Hexawave (漢威)	HW408	1	S1
27	2.4G_BPF	DEA252450BT-2031A1	Multilayer Chip Band Pass Filters for Bluetooth & 2.4GHz W-LAN	TDK		1	F100
28	UP2268	QFN3*3 16 L		UBEC		1	U2
29	UZ2400	QFN-40		UBEC		1	U1
30	0088-V-U-012-B	PCB	4-L,FR-4,G00035			1	

Table 3. BOM list of U-Power500D Module

9. Dot-Power500D Module

9.1. General Introduction

The Dot-Power500D module is derived from the U-Power500D module by attaching a pin-header 2x14 (pitch: 2.54mm) to the interface board. Flexible RF connectors including SMA and SMC are implemented. Through the GSG (ground-signal-ground) interface on the U-Force module, the RF loss is kept to less than 0.3dB. Because of the flexibility offered by the interface boards, Dot-Force module can be readily used for various applications.



Figure 14. Top View of Dot-Power500D Module with Shielding Case

9.2. Pin Header Information

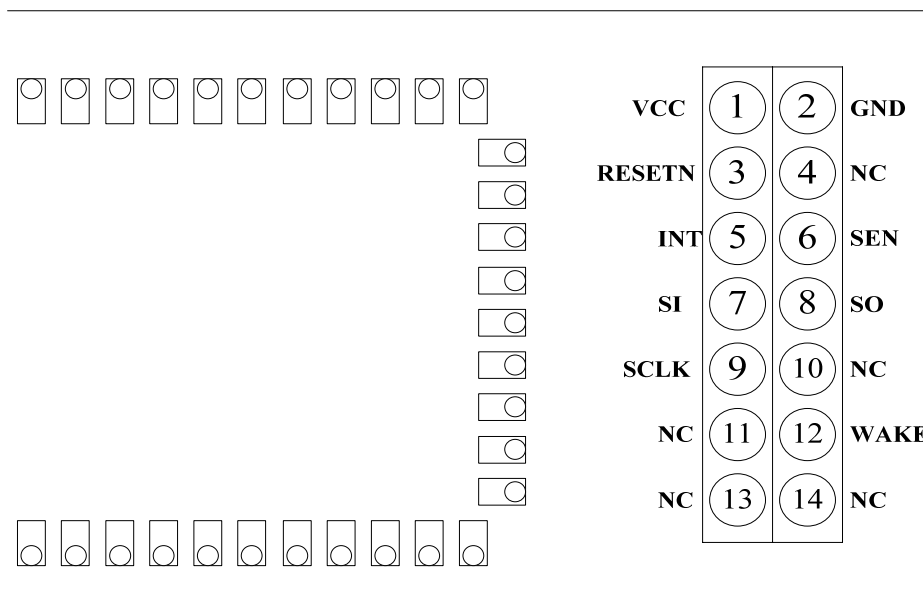


Figure 15. Pin Header Map

9.3. Mechanical Dimension

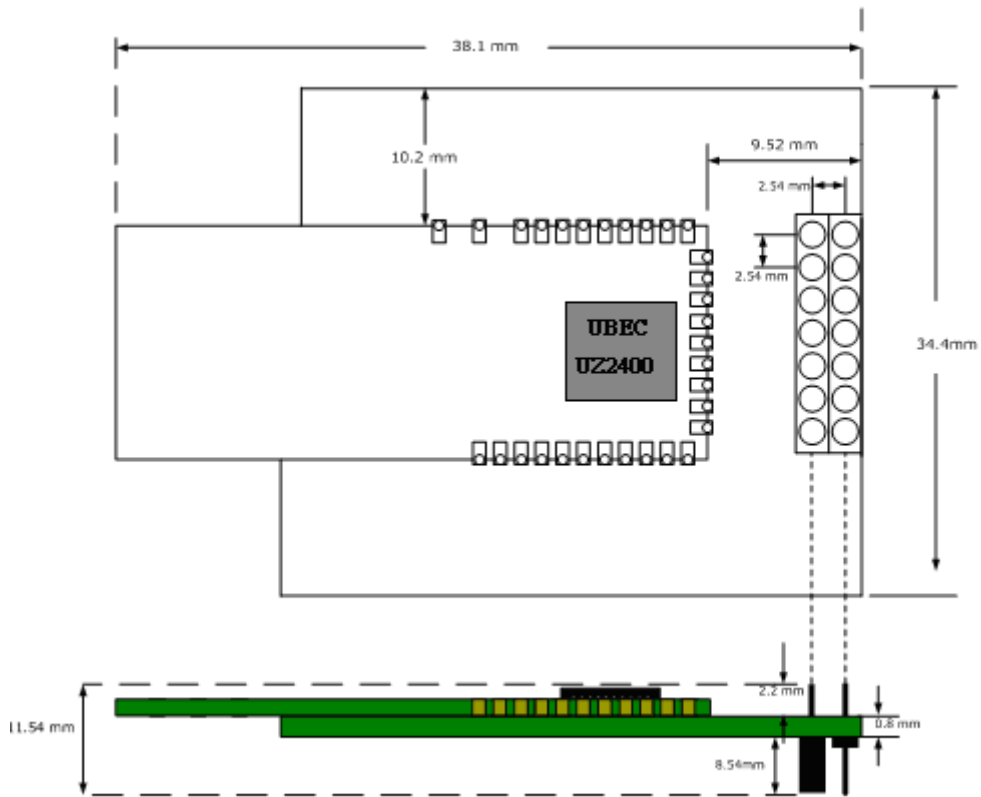


Figure 16. Dimensions of Dot-Power500D Module

Revision History

Revision	Date	Description of Change
0.0	2010/2/26	Initial release.

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