• **1. Placement, Signal and Trace Routing**

• Place the 10/100M magnetic as closely as possible to the DM9000BI / DM9010BI (no more than 20mm) and to the RJ-45 connector.

• Place the termination resistors 50Ω as close as possible to the 10/100M magnetic and the DM9000BI / 9010BI RX± pins and TX± pins. The 50Ω resistors and grounding capacitors of TX± and RX± should be placed near DM9000BI/9010BI (no more than 10mm).

• The 25MHz crystal should not be placed near important signal traces, such as RX± receive pair and TX± transmit pair, band gap resistor, magnetic and board edge.

• Traces routed from the DM9000BI / 9010BI RX± pair to the 10/100M magnetic and the RJ45 connector should run symmetrically, directly, identically, and closely (no more than 2mm). The same rule is applied to traces routed from the DM9000BI / 9010BI TX± pair.

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**Fig. 1-1 Better example for signal and trace routing**

- Do not turn at right angle (90°), turn 45° instead.
- Better: d1 < 2mm, d2 > 3mm, having AGND as a shield is better, d3 > 5mm, having AGND as a shield is better.

**Fig. 1-2 Worse example for signal and trace routing**

- It's worse to turn at right angle (90°).
• It is recommended that RX± receive and TX± transmit traces turn at 45° angle. Do not turn at right angle.

![Better and Worse Trace Examples](image)

• Fig.1-3 Examples for better trace and worse trace

• Avoid using vias in routing the traces of RX± pair and TX± pair.

• The RX± pair, TX± pair, clock, should be routed to have characteristic impedance of 50 Ohm.

• Do not place the DM9000BI / 9010BI RX± receive pair across the TX± transmit pair. Keep the receive pair away from the transmit pair (no less than 3mm). It's better to place ground plane between these two pairs of traces.

• The network interface (see Figure 1-1 and Figure 1-2) does not route any digital signal between the DM9000BI / 9010BI RX± and TX± pairs to the RJ-45. Keep the two pairs away from all the other active signals and the chassis ground.

• It should be no power or ground plane in the area under the network side of the 10/100M magnetic and the area under the RJ-45 connector.

• Any terminated pins of the RJ-45 connector and the magnetic (see Figure 1-1 and Figure 1-2) should be tied as closely as possible to the chassis ground through a resistor divider network 75Ω resistors (no more than 2mm to the magnetic) and a 0.01µF/2KV bypass capacitor.

• The Band Gap resistor should be placed as close as possible to pins 47 and 48 (BGRES, BGRESP) (no more than 3mm). Avoid running any high-speed signal near the Band Gap resistor placement (no less than 3mm from 25MHz XT1 and XT2).
2. DM9000BI / DM9010BI 10Base-T/100Base-TX Application

2-1. DM9000BI Application

Fig. 2-1-1 illustrate the two types of the specific magnetic interconnect and how to connect with DM9000BI. These magnetics are not pin-to-pin compatible. It must be considered when using the DM9000BI in auto-MDIX mode.

Fig. 2-1-1 Application with auto-MDIX transformer (turn ratio 1CT: 1CT)
2-2. DM9010BI Application

Fig. 2-2-1 illustrate the two types of the specific magnetic interconnect and how to connect with DM9010BI. These magnetics are not pin-to-pin compatible. It must be considered when using the DM9010BI in auto-MDIX mode.

Fig. 2-2-1 Application with auto-MDIX transformer (turn ratio 1CT: 1CT)
3. Power Supply Decoupling Capacitors

- Place all the decoupling capacitors for all power supply pins as closely as possible to the power pads of the DM9000BI / DM9010BI (no more than 2.5mm from the above mentioned pins). The recommended decoupling capacitor is 0.1µF or 0.01µF.

- The PCB layout and power supply decoupling should provide sufficient decoupling to achieve the following when measured at the device:
  1. All DVDDs and AVDDs should be within 50mVpp of each other,
  2. All DGNDs and AGNDs should be within 50mVpp of each other.
  3. The resultant AC noise voltage measured across each DVDD/DGND set and AVDD/AGND set should be less than 100mVpp.

- The 0.1-0.01µF decoupling capacitor should be connected between each DVDD/DGND set and AVDD/AGND set and be placed as closely as possible to the pins of DM9000BI / DM9010BI. The conservative approach is to use two decoupling capacitors on each DVDD/DGND set and AVDD/AGND set. One 0.1µF is for low frequency noise, and the other 0.01µF is for high frequency noise on the power supply.

- The AVDD connection to the transmit center tap of the magnetic has to be well decoupled to minimize common mode noise injection from the power supply into the twisted pair cable. It is recommended that a 0.01µF decoupling capacitor should be placed between the center tap AVDD to AGND ground plane. This decoupling capacitor should be placed as closely as possible to the center tap of the magnetic. One 220 µF Capacitor should be connected between each AVDD and AGND. Please see the Fig.3-1, Fig.3-2.

![Diagram](image-url)
Fig. 3-2 the decoupling capacitors for the ground pins of DM9010BI
4. Ground Plane Layout

- Place a single ground plane approach to minimize EMI. Ground plane partitioning can cause increased EMI emissions that could make the network interface circuit not comply with specific FCC part 15 and CE regulations.
- Ground plane need separate analog ground domain and digital ground domain, the analog ground domain and digital ground domain connected line is far away the AGND pins of DM9000BI / DM9010BI (see Fig. 4-1, Fig. 4-3).
- All AGND pins could not directly short each other (see Fig.4-2, Fig.4-4). It must be directly connected to analog ground domain.
- Analog ground domain area is as large as possible.
Fig. 4-3 Ground plane separation for DM9010BI

Fig. 4-4 All AGND pins must be directly connected to analog ground
5. Power Plane Partitioning

- The power planes should be approximately illustrated in Fig. 5-1, Fig. 5-2. No bead is needed to connect two power planes.
- It should separate analog power planes from noisy digital (logic) power planes.

![Fig. 5-1 Power planes partitioning for DM9000BI](image1)

![Fig. 5-2 Power planes partitioning for DM9010BI](image2)
6. Magnetic Selection Guide

- Refer to the following tables 6-1 and 6-2 for 10/100M magnetic sources and specification requirements. The magnetic which meet these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetic specifications before using them in an application. The magnetic listed in the following table are electrical equivalents, but may not be pin-to-pin equivalents.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse Engineering</td>
<td>PE-68515, H1102</td>
</tr>
<tr>
<td>YCL</td>
<td>PH163112, PH163539</td>
</tr>
<tr>
<td>Halo</td>
<td>TG110-S050N2, TG110-LC50N2</td>
</tr>
<tr>
<td>Bel Fuse</td>
<td>S558-5999-W2</td>
</tr>
<tr>
<td>GTS</td>
<td>FC-618SM</td>
</tr>
<tr>
<td>MACOM</td>
<td>HS9016, HS9024</td>
</tr>
</tbody>
</table>

Table 6-1: 10/100M Magnetic Sources

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
<th>Units</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx / RX turns ratio</td>
<td>1:1 CT / 1:1</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Inductance</td>
<td>350</td>
<td>µH (Min)</td>
<td>-</td>
</tr>
<tr>
<td>Insertion loss</td>
<td>1.1</td>
<td>DB (Max)</td>
<td>1 – 100 MHz</td>
</tr>
<tr>
<td>Return loss</td>
<td>-18</td>
<td>DB (Min)</td>
<td>1 – 30 MHz</td>
</tr>
<tr>
<td></td>
<td>-14</td>
<td>DB (Min)</td>
<td>30 – 60 MHz</td>
</tr>
<tr>
<td>Differential to common mode rejection</td>
<td>-40</td>
<td>DB (Min)</td>
<td>1 – 60 MHz</td>
</tr>
<tr>
<td></td>
<td>-30</td>
<td>DB (Min)</td>
<td>60 – 100 MHz</td>
</tr>
<tr>
<td>Transformer isolation</td>
<td>1500</td>
<td>V</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 6-2: Magnetic Specification Requirements
7. Crystal Selection Guidelines

- A crystal can be used to generate the 25.000MHz reference clock instead of an oscillator. The crystal must be a fundamental type, series-resonant, connect to XT1 and XT2, and shunt each crystal lead to ground with a 22pF capacitor as shown in Fig.7-1.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPEC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Fundamental, series-resonant</td>
</tr>
<tr>
<td>Frequency</td>
<td>25.000 MHz +/- 30ppm</td>
</tr>
<tr>
<td>Equivalent Series Resistance</td>
<td>25 ohms max</td>
</tr>
<tr>
<td>Load Capacitance</td>
<td>22 pF typ.</td>
</tr>
<tr>
<td>Case Capacitance</td>
<td>7 pF max.</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>1mW max.</td>
</tr>
</tbody>
</table>

Table 7-1: Crystal Specifications

Figure 7-1 shows the crystal circuit for DM9010BI and DM9000BI.
8. Layout Tracing Notes for MII Signals of DM9010BI to MAC Controller

- The length of the trace routing for the Media Independent Interface (MII) signals should be as short and direct as possible between the DM9010BI and MAC controller (maximum trace distance is shorter than 20cm). These MII signals are as follows,

  CRS, COL, TXD3, TXD2, TXD1, TXD0, TXEN, TXCLK, TXER
  RXER, RXCLK, RXDV, RXD0, RXD1, RXD2, RXD3, MDC, MDIO

- TXD [0-3] and TXCLK length mismatch does not exceed 2cm.
- RXD [0-3] and RXCLK length mismatch does not exceed 2cm.
- All signal trace should be considered to have characteristic impedance of 50 Ohm.