1.1. RX Pointer Restriction

1.1.1. Preface

Because the bus architecture of DM9016 is asynchronous, i.e. the bus does not provide a common timing clock, therefore IOR and IOW are used as asynchronous signals to access data on the bus. As everyone knows, asynchronous bus is sensitive to noise. If any spike on IOR would make the read operation times more then regular one, and this mal-operation could lead chip internal pointer to shift. If the pointer were shifted, processor may not be able to get the right flag on next packet.

1.1.2. Design concept and method

The DM9016 provides a mechanism for bus noise rejection. The DM9016 knows and latches the length of reading packet during processor to do memory data pre-fetch command. The DM9016 uses the latched length as bound to restrict the times of read operation, and then the pointer will no more exceed the boundary.

Furthermore, the DM9016 provides three types of status for showing pointer status after processor read whole packet from DM9016. For instance,

(1). Within buffer:

To indicate the packet in the buffer is not read out completely yet.

(2). End of buffer:

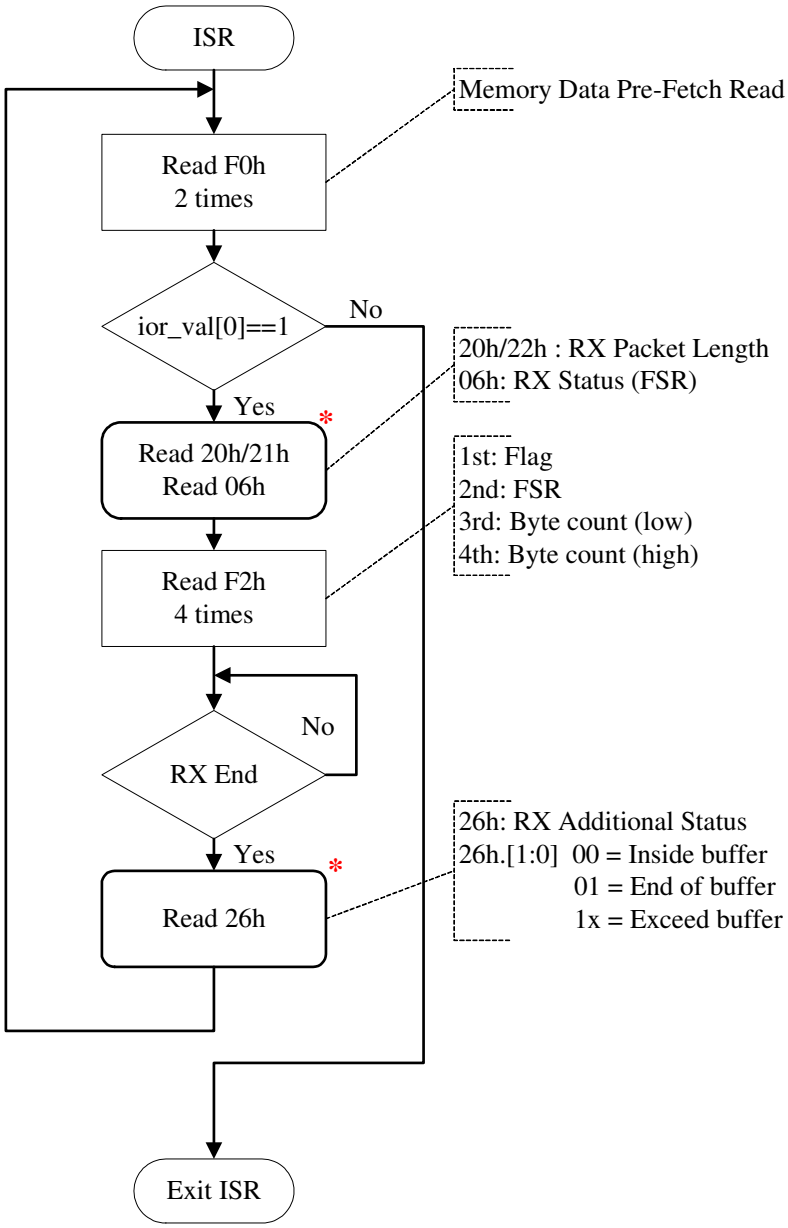
To indicate the packet in the buffer is read out completely.

(3). Without buffer:

To indicate the times of read command exceed the right times, and the reading data may be wrong.

1.1.3. Usage

DM9016 will do the received pointer restriction function automatically. The following flow-chart is the normal receiving procedure of DM9016. There are the two steps, the square with red star sign, are used for debugging.


ISR
Memory Data Pre-Fetch Read
Read F0h
2 times
ior_val[0]==1
No
Yes
20h/22h : RX Packet Length
06h: RX Status (FSR)
*
Read 20h/21h
Read 06h
1st: Flag
2nd: FSR
3rd: Byte count (low)
4th: Byte count (high)
Read F2h
4 times
No
RX End
Yes
26h: RX Additional Status
26h.[1:0] 00 = Inside buffer
01 = End of buffer
1x = Exceed buffer
*
Read 26h
Exit ISR