

US2400

Low Power 2.4 GHz Transceiver IEEE 802.15.4 Standard

PCB Layout Guide AN-2400-90

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1. Introduction

To achieve the best RF performance out of US2400, the 2-Layer PCB layout is recommended as described in this document.



Figure 1: Top view of US2400

2. PCB Layout Rules

Key points to a good PCB Layout:

- (1) PCB:
 - A. Refer to the IC outline drawing, which is given in Datasheet, DS-2400-55, for related US2400 dimensions.
 - B. To realize the best performance out of US2400, the ground plane should be as a continuous plane to the extent possible. Any isolated ground planes should be connected or bridged with wide-width (typically, 10 to 16 mil wide) copper traces.
 - C. Since the bottom side ground of US2400 is divided into a 3-by-3 patch grid, if the ground plane on the PCB, onto which the US2400 is to be mounted, is a whole continuous piece, one can employ a stencil with openings matching the US2400's 3-by-3 patch grid during the solder paste application process. The stencil design is described in more details below.



Figure 2: Bottom view of US2400 and sample PCB



(2) Stencil

- A. Follow the patch location and its size and create a corresponding opening area in the stencil for receiving the solder paste.
- 3. The size of the opening area in the stencil should be around 80% ~ 90% of the US2400 metal patch size. However if the patch size is large than 1 mm², the size of the stencil opening area should be reduced to about 60% ~ 75% of the patch area. This is to prevent undesirable effects arising from the cohesive force of the excessive amount of the molten solder.
- (3) The thickness for the 2-layer FR4 board is 0.8mm. The thickness of the cooper foil is 0.5 ounce. The width of 50 ohm trace is 0.6096mm.
- (4) Reference schematic and layout are attached as Appendix A to this document in Protel 99SE format.

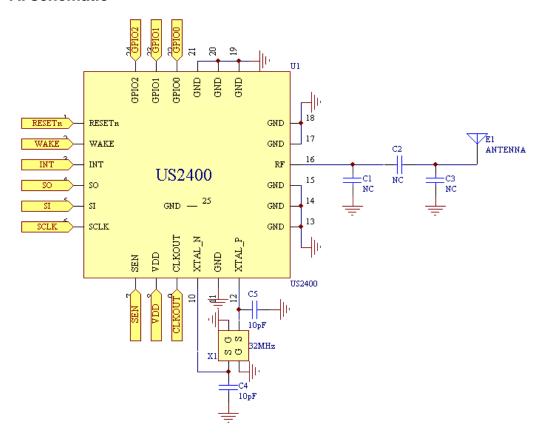
3. Summary

It is highly recommend that users follow this guide to avoid the potential pitfalls when doing the layout design.

4. Attachment

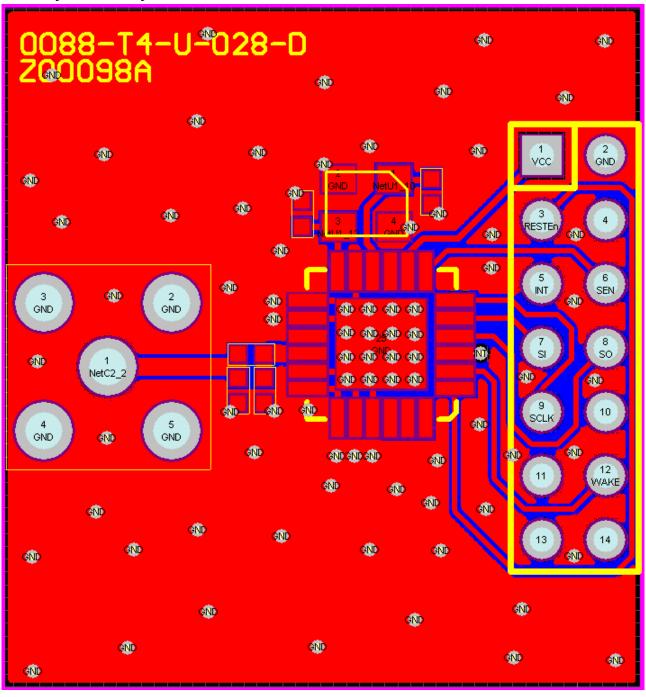
Appendix A: Reference schematic and layout for US2400.

A. schematic



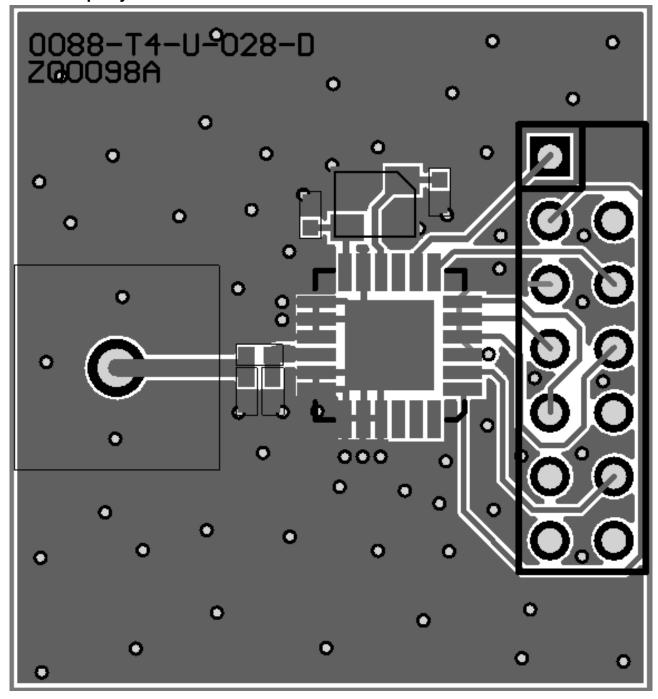


B. 2-Layer PCB Layout



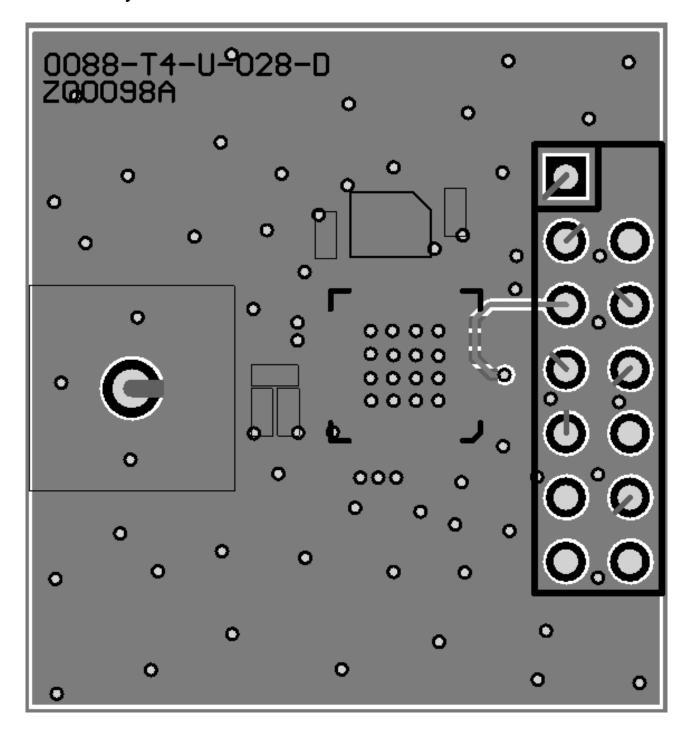


C. PCB Top Layer





D. Bottom Layer





Revision History

Revision	Date	Description of Change
0.0	2011/7/11	Initial release.



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