TITLE: Investigation of UZ2400 Silicon Version D Reset after Repeated Power ON/OFF Switching

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1. Introduction

When the power to a UZ2400 Silicon Version D (Engineering Sample)* module is turned off, the power supply pin VDD of the UZ2400 IC may not be properly discharged if the module does not provide a suitable discharging path for it. For example, this abnormality can be observed if the UZ2400 module is disconnected from the accompanying MCU unit. As a result, the Power-On-Reset function of the UZ2400 may not function properly when the power is turned on again, causing the UZ2400 module to be in a pending state. To resolve this problem, we had investigated the issue and verified that the production version UZ2400 (Mass Production Sample) is free of this problem.

* UZ2400 (Engineering Sample) IC was previously distributed as an engineering sample.

2. UZ2400 (Engineering Sample) Investigation and Results

For this investigation, we have performed both the simulation studies and experimental verifications on the modules that incorporated the UZ2400 (Engineering Sample) and UZ2400 (Mass Production Sample) ICs respectively. The results are summarized as the following.

2.1 Study of the UZ2400 (Engineering Sample) Module Discharging

We used an oscilloscope to measure the abnormal discharging of the power supply pin VDD of the UZ2400 (Engineering Sample) module after the power to the module was turned off. Figure 1 shows a typical voltage discharging diagram in time domain. Right after the power supply VDD is turned off, the VDD voltage will drop immediately to about 0.66V (point t1). But after reaching the time point (t1), the discharging rate becomes very slow. Furthermore the residual VDD voltage has to drop to lower than 0.5V (or thereabouts) before the UZ2400 (Engineering Sample) module will work properly again after the power supply is turned on as discussed in Section 2.2.

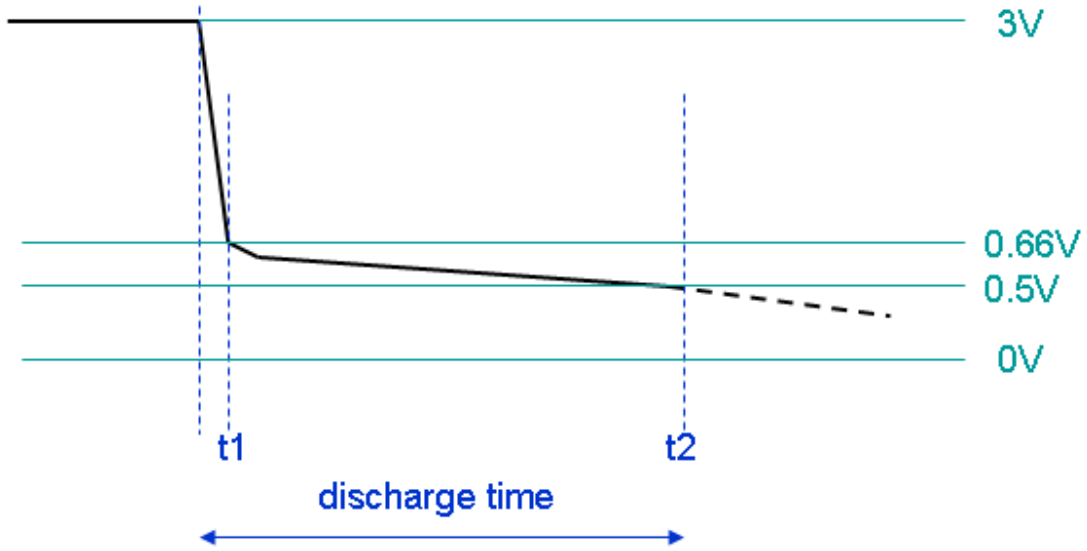

Figure 1. Measured Abnormal Power Supply Discharging at Pin VDD

2.2 UZ2400 (Engineering Sample) Power-On-Reset after Abnormal Discharging

Experimentally we had observed that when the module power supply was turned off and an abnormal discharging occurred, if the residual VDD voltage was not low enough (typically around 0.5V or lower), the power-on-reset function might fail when the power supply was turned on again.

Although this problem can be resolved by adding a shunting resistor between the VDD and the ground, this will induce additional UZ2400 IC leakage current, which is detrimental to the chip performance especially in various sleep modes and therefore not a viable solution.

Another approach is to manually discharge the power supply pin VDD. Again the manual nature renders this approach impractical.

2.3 Analysis and Simulation of UZ2400 (Engineering Sample) Power-On-Reset

The experimental observation was further correlated with a simulation study. Figure 2 shows the voltage simulation of the UZ2400 (Engineering Sample) power-on-reset circuit. A voltage pulse signal which started at 3V was suddenly dropped down to 0.5V and 0.6V respectively and then brought back to 3V after a short duration was applied to the VDD pin. This was to simulate the power on/off/on sequence. The companion power-on-reset voltage waveforms are also displayed. From the simulation results, we observed that a reset signal was generate if the VDD was dropped down to 0.5V. On the other hand, if the VDD only dropped down to 0.6V, no triggering reset signal was produced.

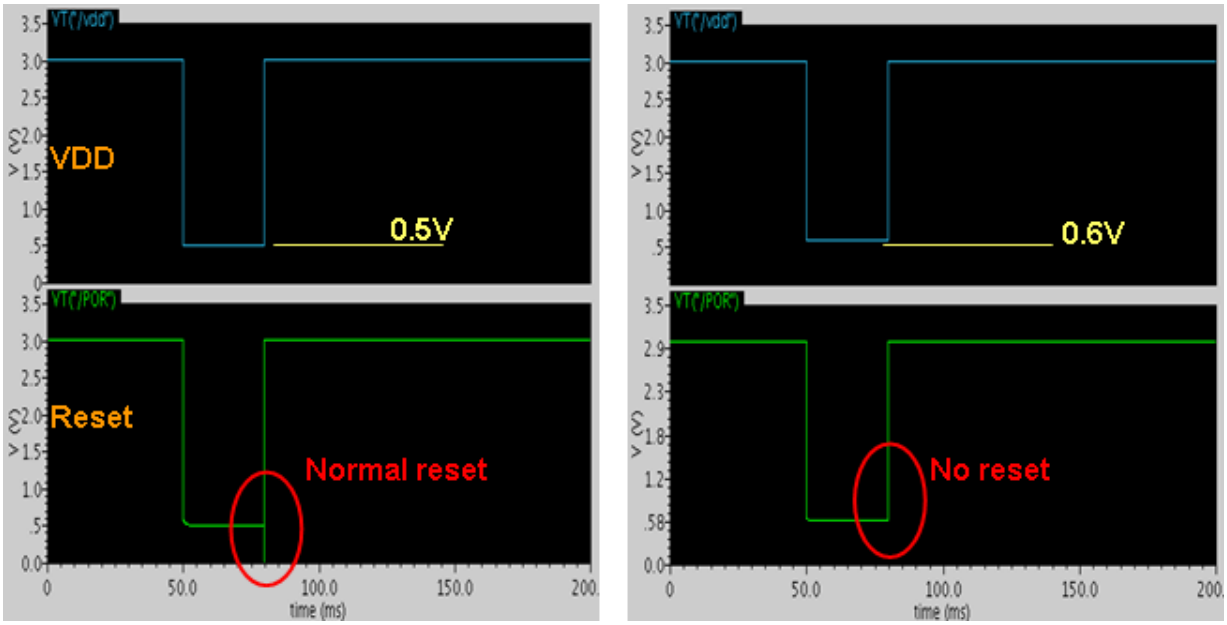

Figure 2. Simulation of the UZ2400 (Engineering Sample) Power-On-Reset after Voltage ON/OFF/ON Applied to VDD Pin.

3. UZ2400 (Mass Production Sample) Investigation and Results

3.1 UZ2400 (Mass Production Sample) Power-On-Reset Improvement

To resolve the discharging issue related to the power on/off cycles, the power-on-reset circuit was modified and implemented in the production version of UZ2400 (Mass Production Sample). Figure 3 shows a similar simulation result of the output of the reset pin. Although the simulated VDD voltage only dropped to 0.6V, the reset voltage waveform is sufficiently low (<< 0.5V) that the UZ2400 (Mass Production Sample) Power-On-Reset can function as designed.

3.2 Experimental Verification of Power-On-Reset Improvement

We had experimentally verified that with the improved Power-On-Reset circuit, UZ2400 (Mass Production Sample) module would no longer suffer the abnormal discharging problem and the chip will reset properly. This is true even when the UZ2400 (Mass Production Sample) is under rapid power ON/OFF/ON toggling.

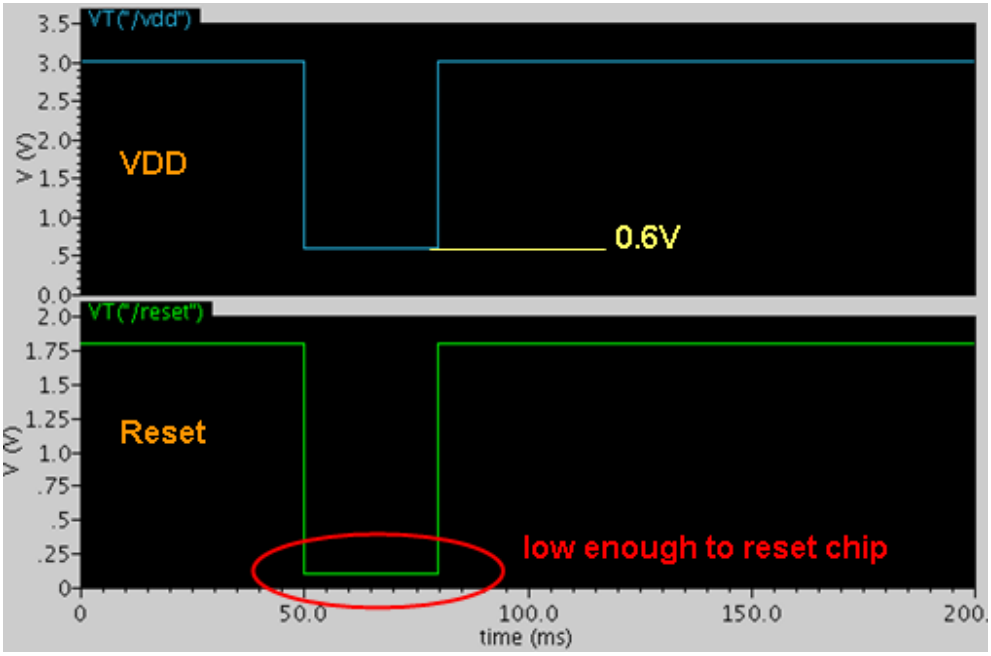

Figure 3. Simulation result of the modified power-on-reset circuit.

4. Summary

The power-on-reset problem detected on UZ2400 Silicon Version D (Engineering Sample) was identified to be related to an abnormal VDD pin voltage discharging after the power to the module is turned off. With the improved power-on-reset circuit, the production version UZ2400 (Mass Production Sample) is free of this problem.