

UZ2400

Silicon Version D

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

U-ForceD Module Application Note AN-2400-62

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Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

1. General Information

The U-ForceD module is an IEEE 802.15.4 compliant solution that satisfies the requirements of low-cost and low-power wireless applications. The module, containing UBEC's UZ2400 silicon version D and other necessary components, operates in the ISM 2.4 GHz frequency band. The corresponding MCU can access various UZ2400 internal subunits, such as registers, FIFOs, and security key table, via a 4-wire SPI bus. Its small form factor saves the valuable board spaces and provides a reliable delivery of critical data between the devices.

2. Features

- ❑ 2.4GHz IEEE 802.15.4 Compliant
- ❑ 1.8~3.6V Operation
- ❑ Sleep Current: 2.4µA, typical
- ❑ Effective Distance: 100 meters (line of sight, environment dependent, typical)
- ❑ PCB Antenna
- ❑ Additional GSG (ground-signal-ground) Interfaces Provided
- ❑ Receiver Sensitivity: -95dBm, typical
- ❑ Tx Output Power: 0dBm, typical
- ❑ Tx Current Consumption: DCDC OFF 23.2mA ,DCDC ON 17.5mA, typical
- ❑ Rx Current Consumption: DCDC OFF 20.4mA ,DCDC ON 16.2mA, typical
- ❑ Dimension: 31.5mmx14mmx1.7mm
- ❑ Compliant with EN300 328 V1.7.1

3. Pin Configuration

3.1. Pin Assignment

Top view of a U-ForceD module and its pin allocation map are shown in Figure 1 and Figure 2 respectively.

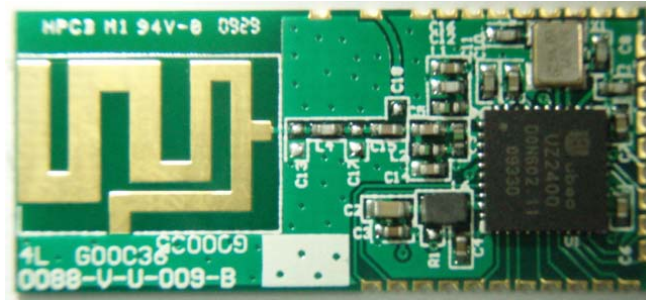


Figure 1. Top View of U-ForceD Module

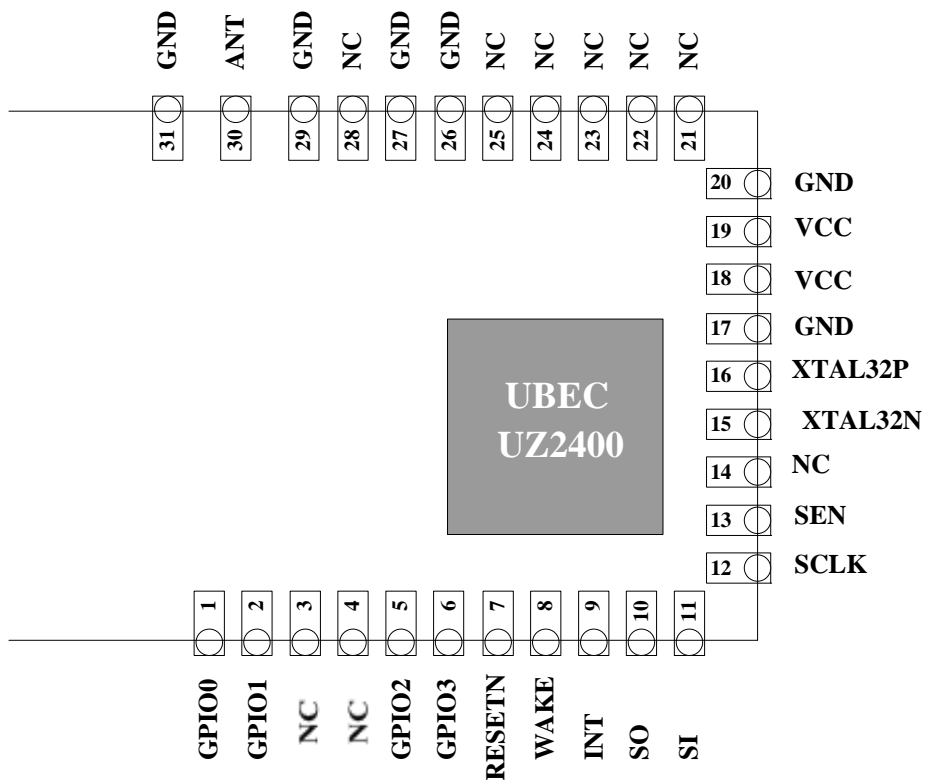


Figure 2. Pin Allocation

3.2. Pin Description

Pin type abbreviation: A = Analog, D = Digital, I = Input, O = Output, P = Power, G = Ground

Pin	Name	Type	Description
1	GPIO0	DIO	General purpose digital I/O, also used as an external PA enable
2	GPIO1	DIO	General purpose digital I/O, also used as an external TX/RX switch control
3	NC		No connection
4	NC		No connection
5	GPIO2	DIO	General purpose digital I/O, also used as an external TX/RX switch control
6	GPIO3	DIO	General purpose digital I/O
7	RESETN	DI	Global hardware reset pin, active low
8	WAKE	DI	External wake up trigger, active high / low can be programmable.
9	INT	DO	Interrupt pin to micro-processor: Level trigger, Hi / Low programmable
10	SO	DIO	Serial interface data output from UZ2400 or I2C clock
11	SI	DIO	Serial interface data input to UZ2400 or I2C data in/out
12	SCLK	DI	Serial interface clock
13	SEN	DI	Serial interface enable
14	NC		No Connection
15	XTAL32N	AI	32 kHz Crystal input (-) for internal RTC used
16	XTAL32P	AI	32 kHz Crystal input (+) for internal RTC used
17	GND	G	Ground
18	VCC	PI	Power supply
19	VCC	PI	Power supply
20	GND	G	Ground
21~25	NC		No connection
26,	GND	G	Ground
27	GND	G	Ground
28	NC		No connection
29	GND	G	Ground
30	ANT	AIO	Antenna Port
31	GND	G	Ground

Table 1. Pin Assignment

4. Electrical Specifications

Test conditions: $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$

ITEM	Condition	Specification			Unit
		Min.	Typ.	Max.	
Frequency		2405		2480	MHz
Supply voltage(1)		1.8	3	3.6	V
TX Current consumption	$P_{out}(UZ2400)=0\text{dBm}$		17.5		mA
RX Current consumption			16.2		mA
TX Output power	$P_{out}(UZ2400)=0\text{dBm}$		0		dBm
TX EVM	$P_{out}(UZ2400)=0\text{dBm}$		12		%
RX sensitivity	PER $\leq 1\%$ O-QPSk 250kbps		-95		dBm
Communication Range	Throughput $>120\text{kbps}$ at 250kbps data rate, LOS		100		m

Note 1: DC-DC Converter should be bypassed if supply voltage is below 2.4V.

Table 2. Electrical Specifications

For detail electrical characteristic of the UZ2400 chip, please refer to UZ2400 Datasheet (Document No.: DS-2400-51).

4.1. TX Output Power

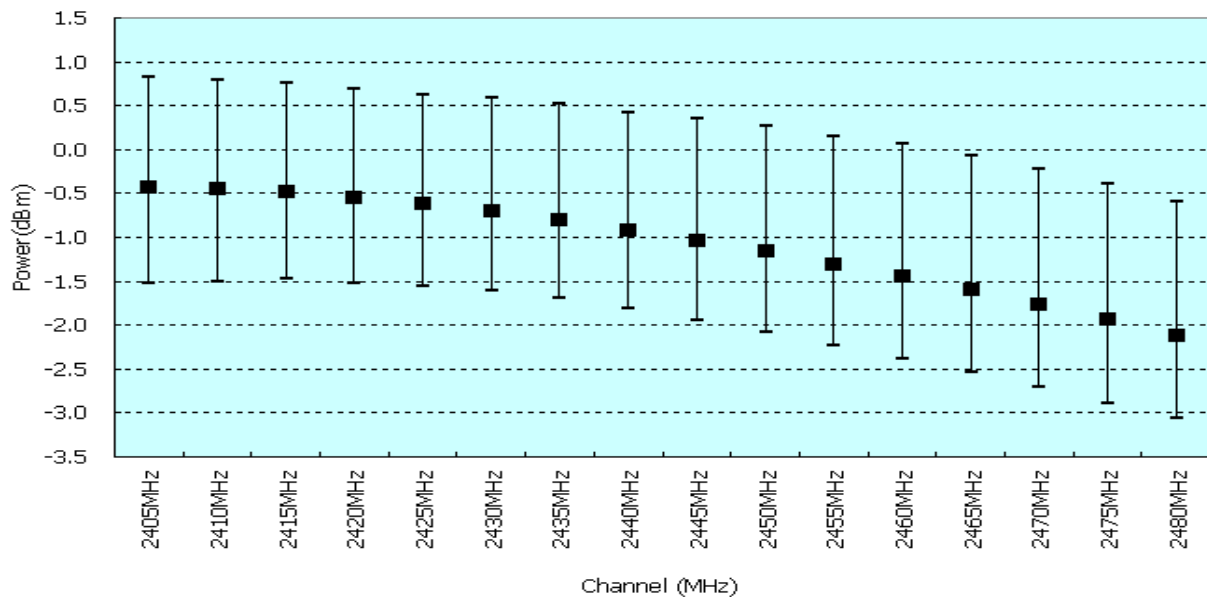


Figure 3. Typical TX Output Power with DC/DC-on Mode

4.2. TX EVM

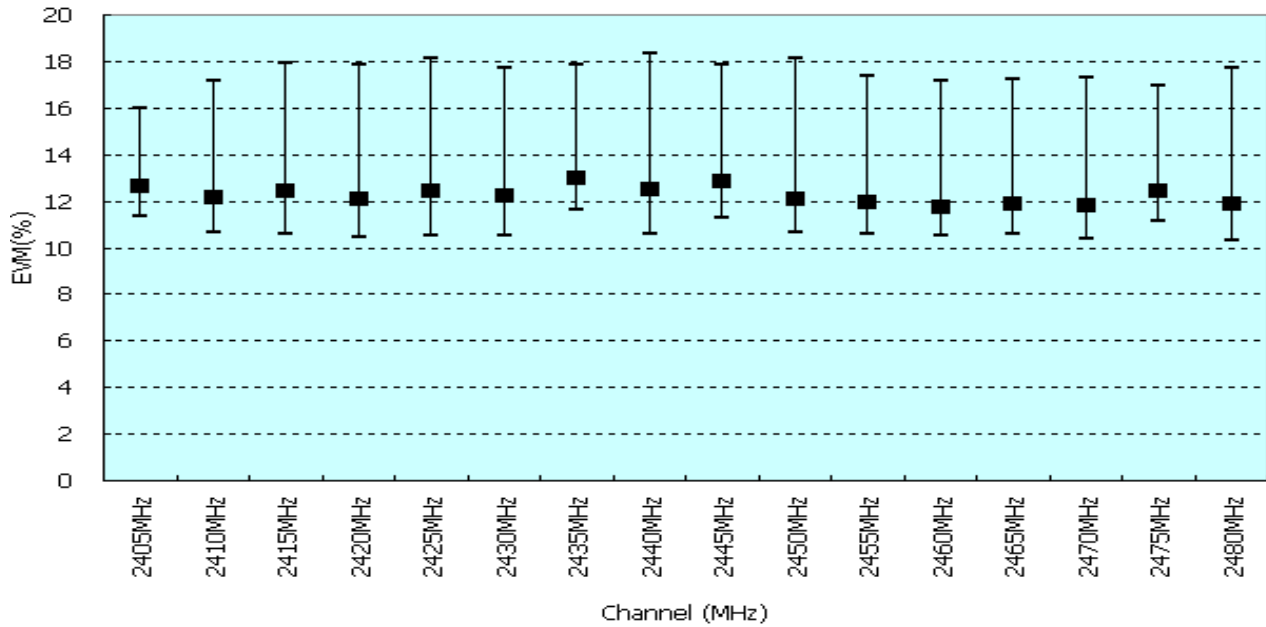


Figure 4. Typical TX EVM with DC/DC-on Mode

4.3. RX Sensitivity

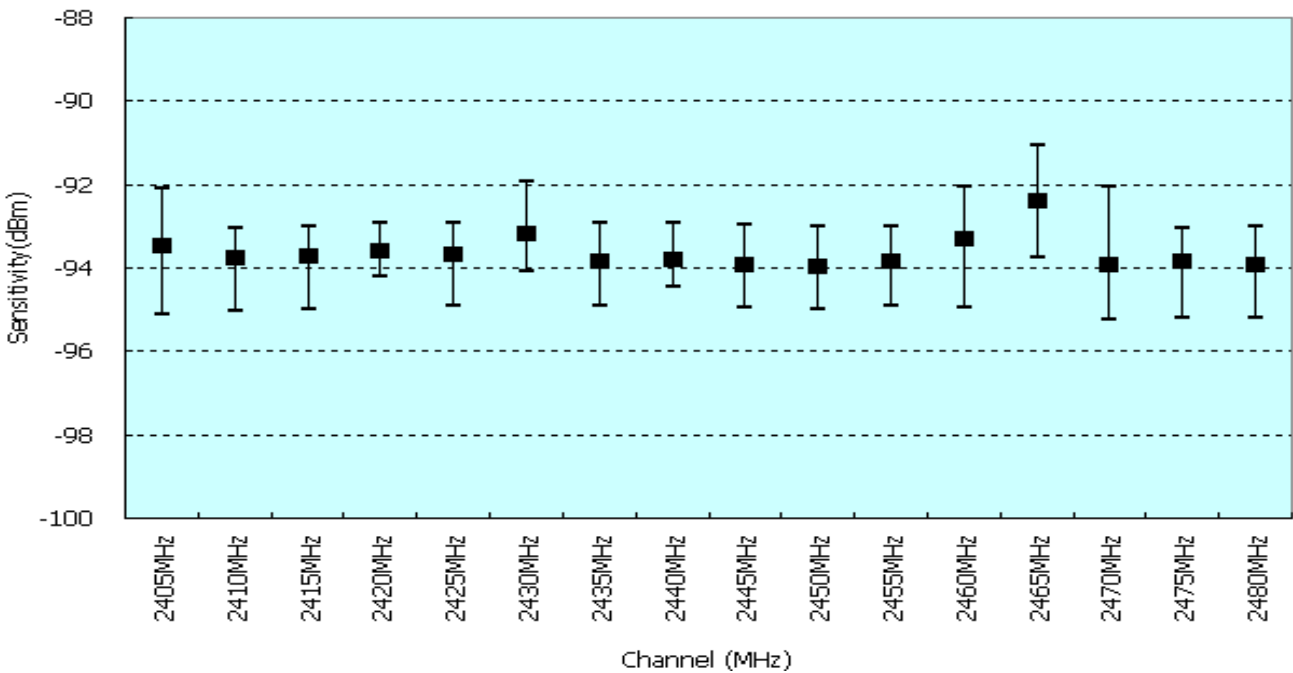


Figure 5. Typical RX Sensitivity with DC/DC-on Mode

4.4. Antenna Radiation Patterns

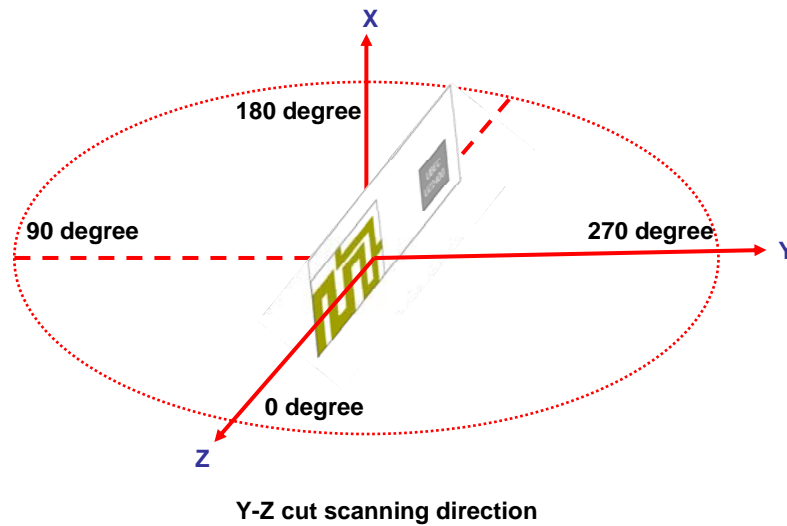


Figure 6. 3-dimension coordinate Y-Z plan

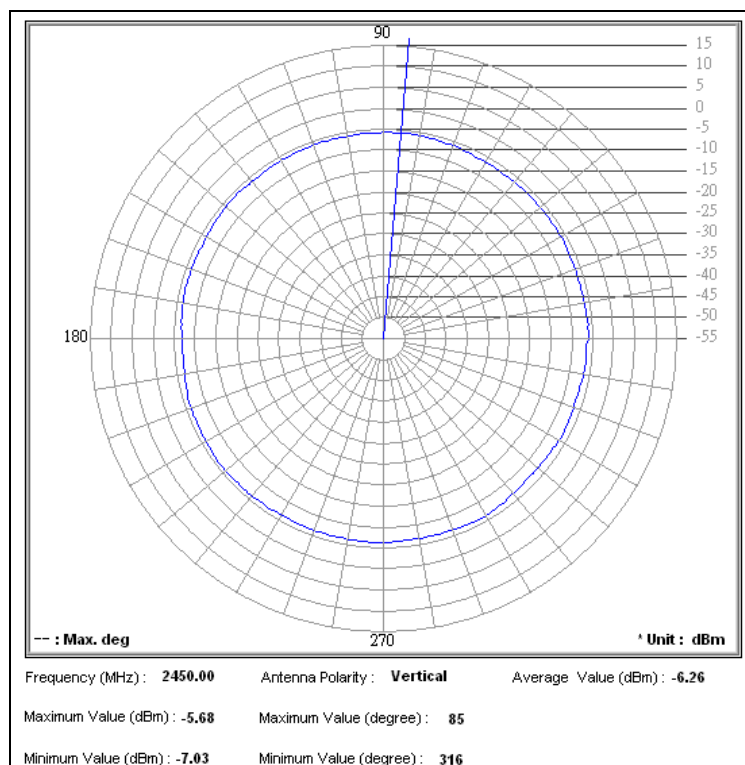


Figure 7. Y-Z Plan, Vertical Polarization @ 2.45GHz

5. Recommended Antenna Placement

- (1) Antenna should be put on the edge of the system.
- (2) Be sure that there are no obstacles (components and ground) in the radiation direction.
- (3) Do not put any ground plane and/or circuit beneath the antenna region for the system boards.

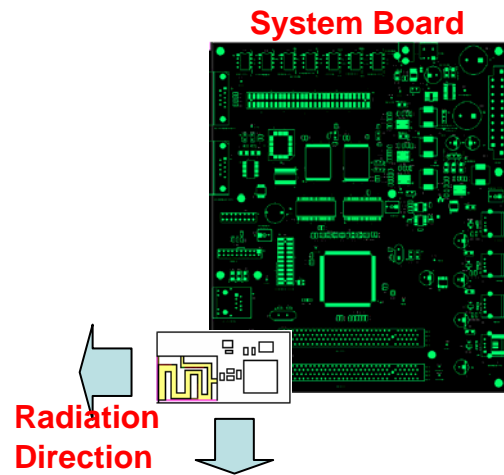


Figure 12. Recommended Antenna Placement

6. Register Initial Setting

Refer to register initial setting of the UZ2400 Datasheet (Document No.: DS-2400-51).

7. Schematic

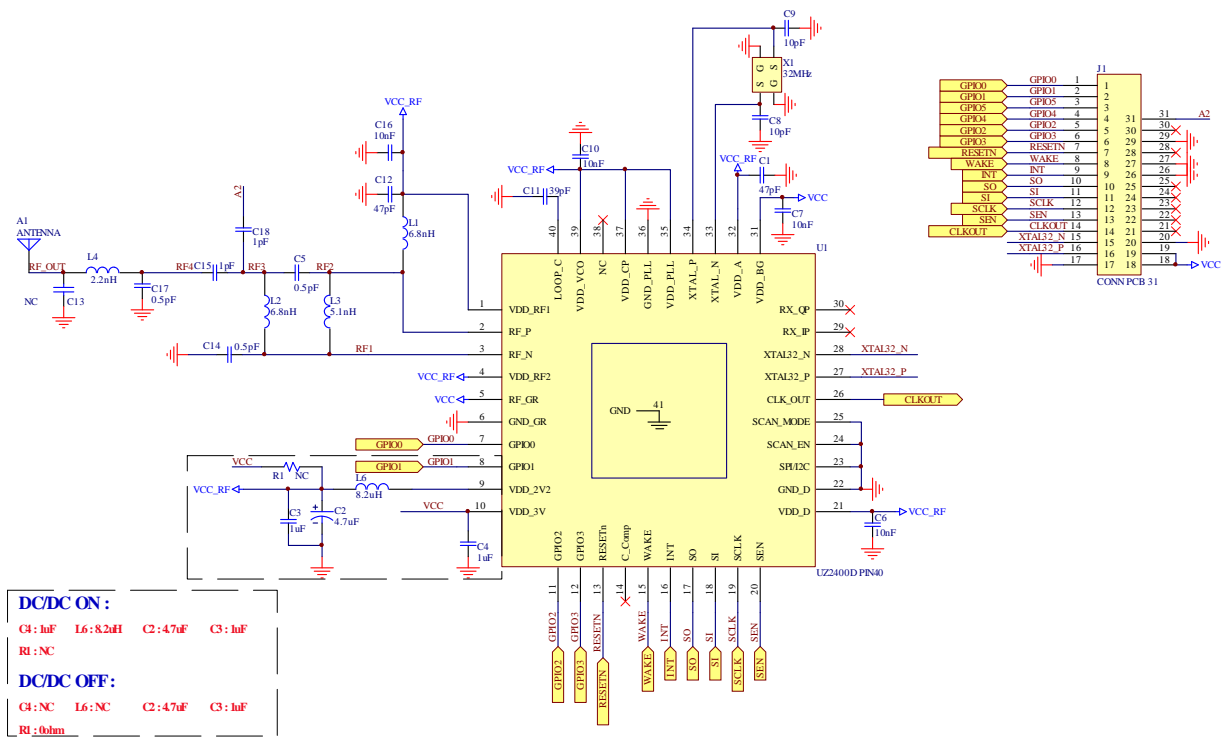


Figure 13. Schematic of U-Forced Module

8. PCB Layout

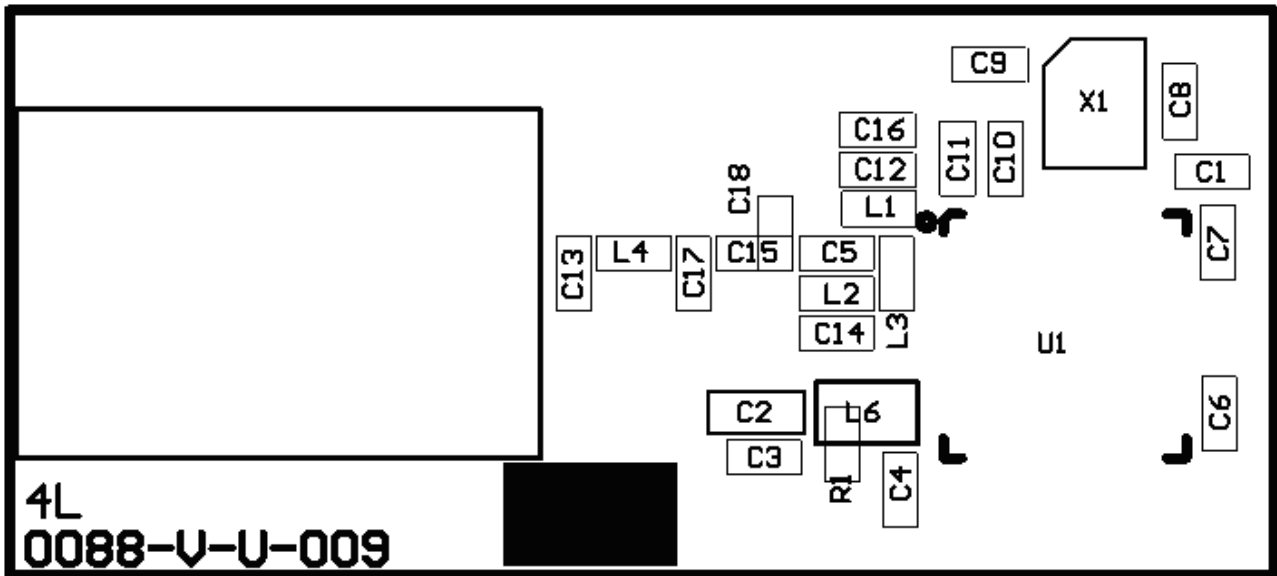


Figure 14. Top Overlay

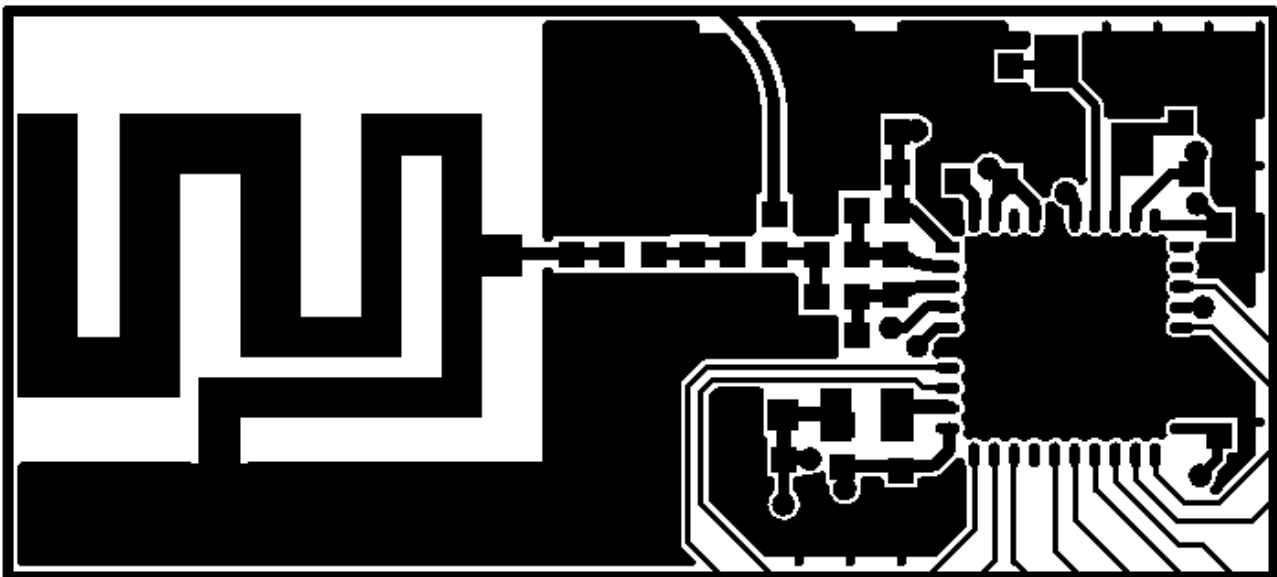


Figure 15. Top Layer (Signals)

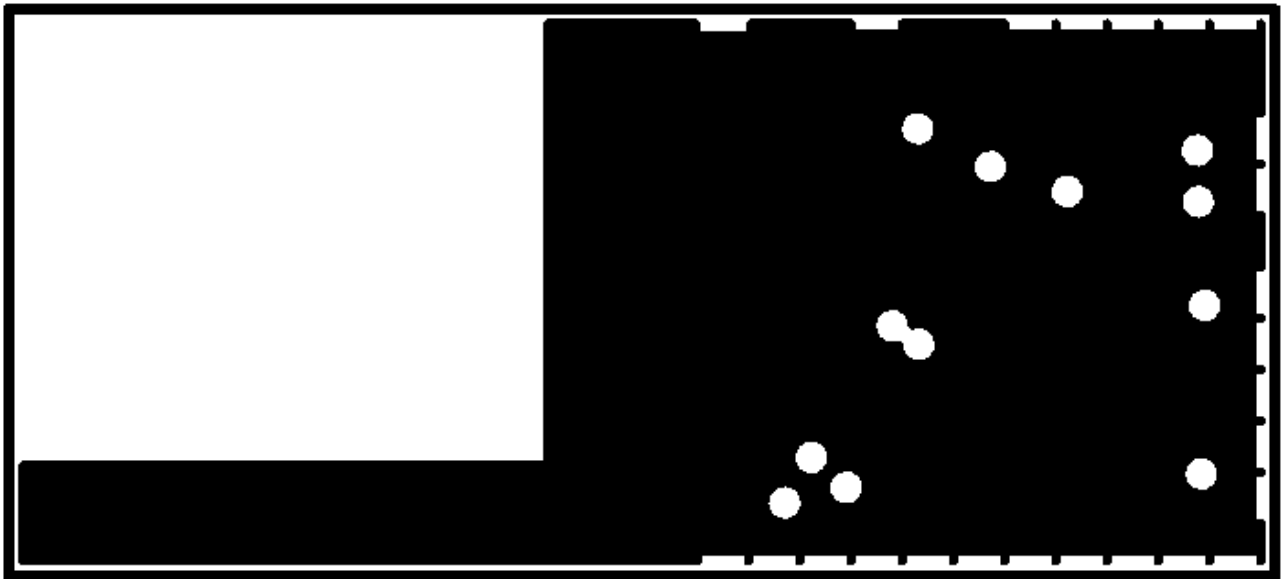


Figure 16. Ground plane

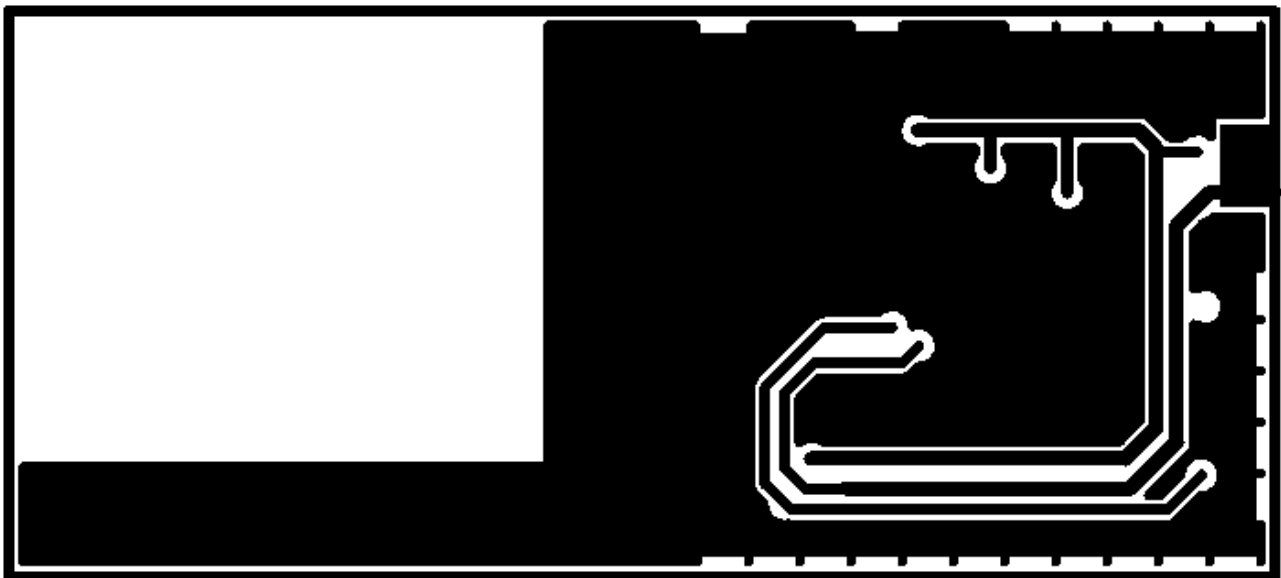


Figure 17. Power plane

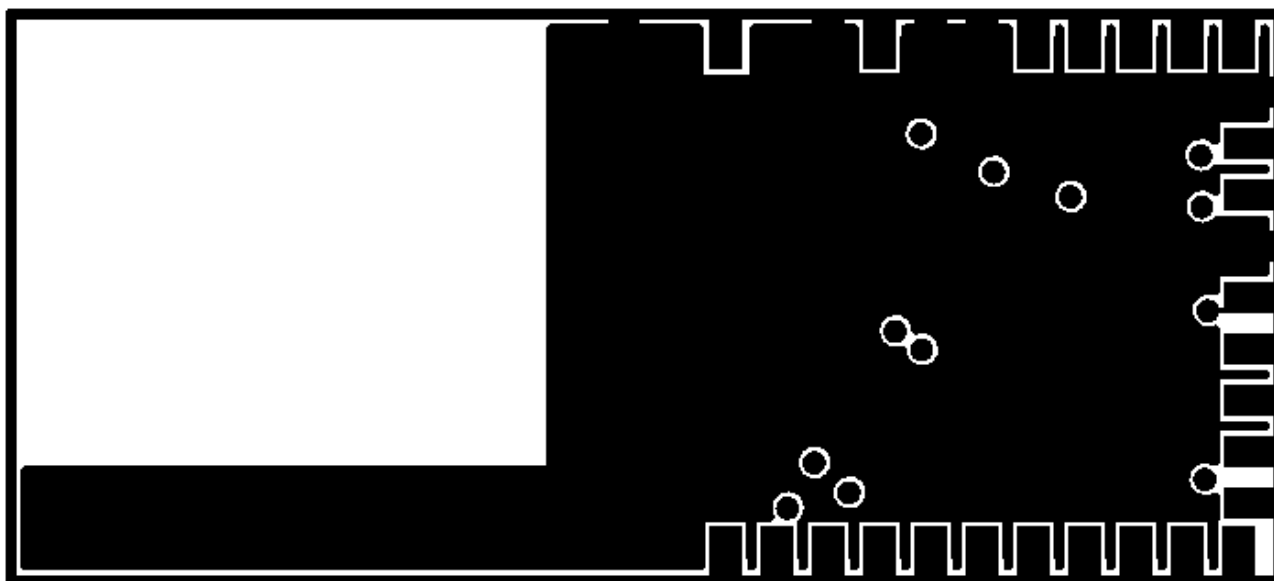


Figure 18. Bottom Layer

9. BOM List

Item	Part name	Footprint	Tolerance	Manufacturer	Manufacturer Part No.	Qty	Reference
1	0.5pF	0402	50V NPO $\pm 0.25\text{pF}$	C CHIP Yageo	CC0402CRNPO9BNR50	2	C5 C14
2	1pF	0402	50V NPO $\pm 0.25\text{pF}$	C CHIP Yageo	CC0402CRNPO9BN1R0	1	C15
3	1uF	0402	6.3V Y5V -20~+80%	C CHIP Yageo	CC0402ZRY5V5BB105	2	C3 C4
4	4.7uF	0603	10V X5R $\pm 10\%$	L chip Murata	GRM188R61A475K	1	C2
5	8.2uH	0806	$\pm 20\%$	L chip Murata	LQH2MCN8R2M02	1	L6
6	6.2nH	0402	$\pm 0.3\text{nH}$	L chip Murata	LQG15HN6N2S02	1	L3
7	5.1nH	0402	$\pm 0.3\text{nH}$	L chip Murata	LQG15HN5N1S02	2	L1 L2
8	10nF	0402	16V Y5V -20~+80%	C CHIP Yageo	CC0402ZRY5V7BB103	4	C6 C7 C10 C16
9	10pF	0402	50V NPO $\pm 5\%$	C CHIP Yageo	CC0402JRNPO9BN100	4	C8 C9 L4
10	39pF	0402	50V NPO $\pm 5\%$	C CHIP Yageo	CC0402JRNPO9BN390	1	C11
11	47pF	0402	50V NPO $\pm 5\%$	C CHIP Yageo	CC0402JRNPO9BN470	2	C1 C12
12	0R	0402	1/16W $\pm 5\%$	R chip, Yageo	RC0402JR-070R	1	R1
13	CRYSTAL32MHz	CX_101F	15ppm/8pF/3.2*2.5mm	NDK	N3225SA	1	X1
14	UZ2400D PIN40			UBEC		1	U1
15	0088-V-U-009-B2	PCB	4-L,FR-4,G00036	UBEC		1	

Table 3. BOM List of U-Forced Module

11. Dot-ForceD Module

11.1. General Introduction

The Dot-ForceD module is derived from the U-ForceD module by attaching a pin-header 2x7 (pitch: 2.54mm) to the adaptor board, on which SMA connector is implemented.

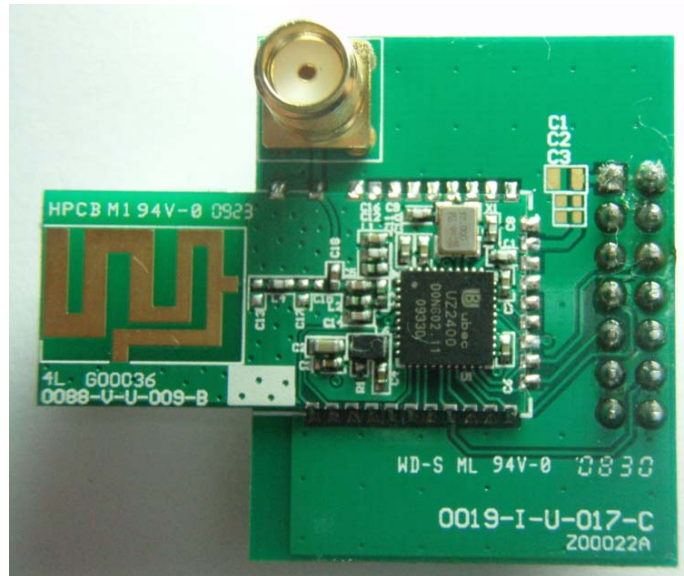


Figure 21. Top View of Dot-ForceD Module

11.2. Pin header information

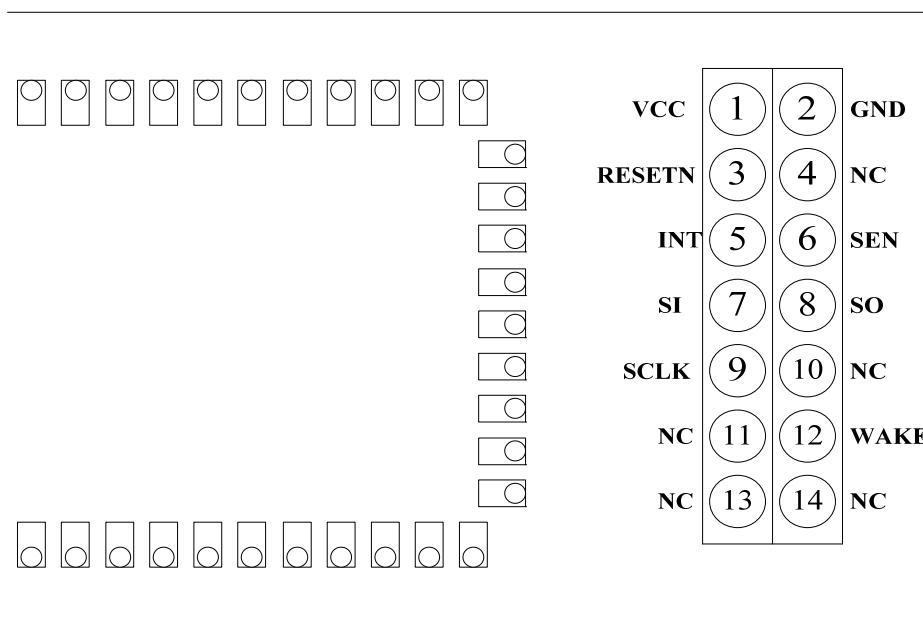


Figure 22. Pin Header Map

11.3. Dot-ForceD Module Dimension

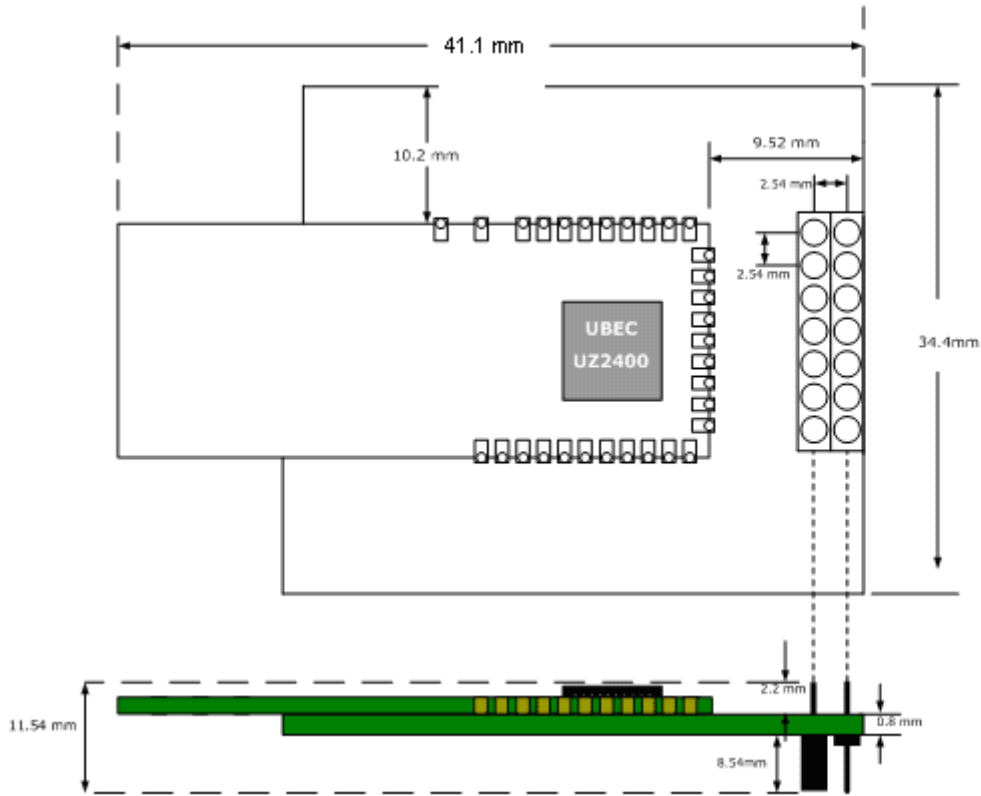


Figure 23. Dimensions of Dot-ForceD Module

Revision History

Revision	Date	Description of Change
0.0	2009/11/17	Initial release.
0.1	2010/04/02	Modify dimension

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