industrial

GOODRAM Industrial
DDR5 UDIMM 288pin

standard temperature

DATASHEET

Document number:
Version: 1.0
Date: May 2023

Wilk Elektronik S.A.
Mikołowska 42
43-173 Łaziska Górne, Poland
Tel.: +48 32 736 90 00, Fax.: +48 32 736 90 01
E-mail: sales@goodram.com

This document is subject to change without any notice.

Please contact your Wilk Elektronik S.A. sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Wilk Elektronik S.A. assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.

REVISION HISTORY

VERSION	CHANGES	DATE
1.0	Initial release	18.05.2023

TABLE OF CONTENTS

PRODUCT OVERVIEW

Module Form Factor	288-pin, unbuffered small-outline dual in-line memory module (UDIMM)
Interface	DDR5, JEDEC compliant JESD79-5
Capacity	8GB – 32GB
Fast Data Transfer Rates	PC5-4800 @4800 MT/s; PC5-5600 @5600 MT/s
DRAM IC Type	1Gx16 , 2Gx8
Power Supply	VIN Bulk = 5V; VDD/VDQQ = 1.1V; VPP = 1.8V
On-Die ECC Support	YES
ECC Support	NO
Registered	NO
Thermal Sensor	YES (integrated in SPD5 Hub Device)
Additional Thermal Sensor	NO
Temperature range	Operating: 0°C ~ +85°C; Storage: -40°C ~ +100°C
Gold edge contacts	YES
RoHS compliant	YES

PRODUCT DETAILS

General Description

DDR5 SDRAM is a high-speed dynamic random-access memory. To ease transition from DDR4 to DDR5, the introductory density (8Gb) shall be internally configured as 16-bank, 8 bank group with 2 banks for each bank group for x4/x8 and 8-bank, 4 bank group with 2 banks for each bank group for x16 DRAM. When the industry transitions to higher densities (=>16Gb), it doubles the bank resources and internally be configured as 32-bank, 8 bank group with 4 banks for each bank group for x4/x8 and 16-bank, 4 bank group with 4 banks for each bank group for x16 DRAM.

DDR5 SDRAM uses a 16n prefetch architecture to achieve high-speed operation. The 16n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR5 SDRAM consists of a single 16n-bit wide, eight clock data transfer at the internal DRAM core and sixteen corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR5 SDRAM are burst oriented, start at a selected location, and continue for a burst length of sixteen or a ‘chopped’ burst of eight in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command.

SPD5 Hub Device

The SPD5 Hub device family contains 1024 bytes of non-volatile memory arranged as 16 blocks of 64 bytes per block. Each block may optionally be write protected via software command.
The SPD5 Hub device operate from 1.8 V nominal power supply input. SPD5 Hub devices are intended to interface to I2C/I3C Basic buses which have multiple devices on a shared bus and must be uniquely addressed with fixed addressing on the same bus.
All SPD5 Hub devices respond to specific pre-defined I2C/I3C Basic device select codes on a host interface bus. The SPD5118 devices also incorporate a second local I2C/I3C Basic bus and pass through of commands from the host bus onto the local bus for addressing of I2C/I3C Basic devices on the local bus (Hub function). The SPD5118 device incorporates thermal sensing capability which is controlled and read over I2C/I3C Basic bus.

PMIC Device

The PMIC5100 is designed for typical DDR5 SODIMM as well as DDR5 UDIMM. The PMIC features three step down switching regulators and two LDO regulators . The PMIC is powered from VIN_Bulk input for the entire PMIC including the switching regulators and LDO output regulators. The PMIC supports selectable interface (I2C or I3C Basic) to fit various application environment.

On-Die ECC

On-Die ECC is a new feature designed to correct bit errors within the DRAM chip. As DRAM chips increase in density through shrinking wafer lithography, the potential for data leakage increases. On-die ECC mitigates this risk by correcting errors within the chip, increasing reliability and reducing defect rates. This technology cannot correct errors outside of the chip or those that occur on the bus between the module and memory controller housed within the CPU. On reads, the DRAM corrects any single-bit errors before returning the data to the memory controller. The DRAM shall not write the corrected data back to the array during a read cycle. On writes, the DRAM computes ECC and writes data and ECC bits to the array. If the external data transfer size is smaller than the 128 data bits code word (x4 devices), then DRAM will have to perform an internal 'read-modify-write' operation. The DRAM will correct any single-bit errors that result from the internal read before merging the incoming write data and then re-compute 8 ECC Check bits before writing data and ECC bits to the array. In the case of a x8 and x16 DDR5, no internal read is required.

(*) Source: JEDEC JESD79-5, JESD300-5, JESD301-2

PART NUMBERS AND TIMING PARAMETERS

PART NUMBER	MODULE DENSITY	CONFIGURATION	MODULE BANDWITH	MEMORY CLOCK / DATA RATE	CLOCK CYCLES (CL-tRCD-tRP)
GR5D8G480S6C	8GB	1Gx16 SR	38.4 GB/s	0.416ns/4800 MT/s	40-39-39
GR5D16G480S8C	16GB	2Gx8 SR	38.4 GB/s	0.416ns/4800 MT/s	40-39-39
GR5D32G480D8C	32GB	2Gx8 DR	38.4 GB/s	0.416ns/4800 MT/s	40-39-39
GR5D8G560S6C	8GB	1Gx16 SR	44.8 GB/s	0.357ns/5600 MT/s	46-46-46
GR5D16G560S8C	16GB	2Gx8 SR	44.8 GB/s	0.357ns/5600 MT/s	46-46-46
GR5D32G560D8C	32GB	2Gx8 DR	44.8 GB/s	0.357ns/5600 MT/s	46-46-46

SR – Single Rank
DR – Dual Rank

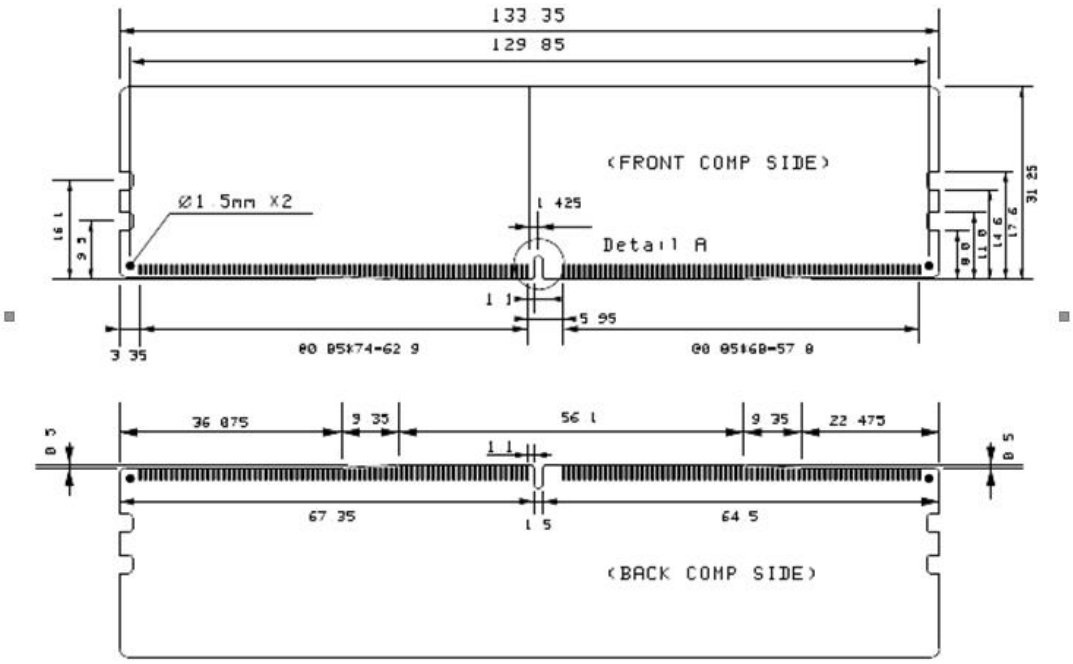
C – standard

ADDRESSING

PARAMETER	8GB SR	16GB SR	32GB DR
Row address	64K (R0-R15)	64K (R0-R15)	64K (R0-R15)
Column address	1K (C0-C9)	1K (C0-C9)	1K (C0-C9)
Device bank group address	4 (BG0-BG1)	8 (BG0-BG2)	8 (BG0-BG2)
Device bank address per group	4 (BA0-BA1)	4 (BA0-BA1)	4 (BA0-BA1)
Device configuration	16Gb (1Gbx16), 16 banks	16Gb (2Gbx8), 32 banks	16Gb (2Gbx8), 32 banks
Module rank address	1 (CS0_n)	1 (CS0_n)	2 (CS0_n, CS1_n)

PHYSICAL DIMENSION

Dimensions: 133.35mm (L) * 31.25mm (W)



Note:
1. All dimensions are in millimeters (inches). MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to JEDEC document for additional design dimensions.

STANDARDS & REFERENCES

The following table is to list out the standards that have been adopted for designing the product.

STANDARD USED	ACRONYM/SOURCE
RoHS	Restriction of Hazardous Substances Directive
CE	Consumer electronics certification; please contact us for further information.

SAFETY PRECAUTIONS

Do not bend, crush, drop or place heavy objects on top of the Product. Do not use tweezers, pliers or similar items that could damage the Product. Take particular care when inserting or removing the Product. Stop using the Product when the Product does not work properly. Failure to follow these instructions could result in fire, damage to the Product and/or other property, and/or personal injury including burns and electric shock.

Keep out of reach of small children. Accidental swallowing may cause suffocation or injury. Contact a doctor immediately if you suspect a child has swallowed the Product.

Do not directly touch the interface pins, put them in contact with metal, strike them with hard objects or cause them to short. Do not expose to static electricity.

Do not disassemble or modify the Product. This may cause electric shock, damage to the Product or fire.

NOTES ON USAGE

The Product contains nonvolatile semiconductor memory. Do not use the Product in accordance with a method of usage other than that written in the manual. This may cause the destruction or loss of data.

To protect against accidental data loss, you should back up your data frequently on more than one type of storage media. Wilk Elektronik S.A. assumes no liability for destruction or loss of data recorded on the Card for any reason.

When used over a long period of time or repeatedly, the reading, writing and deleting capabilities of the Product will eventually fail, and the performance speed of the Product may decrease below the original speed specific to the Product's applicable class.

If the Product is to be transferred or destroyed, note that the data it contained may still be recoverable unless it is permanently deleted by third-party deletion software or similar means beforehand.

Product is intended for use in general electronics applications and selected industrial applications and any other specific applications as expressly stated in this document. Product is neither intended nor warranted for use in equipment or systems where failure may cause loss of human life, bodily injury, serious property damage or serious public impact (“Unintended Use”). Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment or equipment used to control combustions or explosions. Do not use Product for Unintended Use unless specifically permitted in this document.

Wilk Elektronik S.A. does not make any warranty, express or implied, with respect to this document, including as to licensing, Non-infringement, merchantability or fitness for a particular purpose.