Silicon Power
INDUSTRIAL

Industrial

DRAM

DDR5 SODIMM Series

Datasheet

Specifications Overview

- **Capacity**
- 8GB, 16GB, 32GB, 48GB
- **Form Factor**
  - DDR5 SODIMM
- **Performance**
  - 4800 = 38.4 GB/s
  - 5600 = 44.8 GB/s
- **Temperature Range**
  - Operation temperature:
    Normal temperature: -20°C to +95°C
    Wide temperature: -40°C to +105°C
- **Power Consumption**
  - Supply Voltage: DC +1.1V ± 5%
- **Compliant Specifications**
  - RoHS

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Table of Contents

List of Table

Revision History

Revision	Date	Major Changes
1.0	2022/08	First release
1.1	2022/09	Add DDR5-5600
1.2	2023/06	Add DDR5 8GB (1Gx16) Update IDD Specification
1.3	2023/10	Add Hynix Solution Update Normal temperature to -20°C Update IDD Specification
1.4	2023/12	Update temperature
1.5	2024/09	Adjust Format Add DDR5 48GB (3Gx8)
1.6	2024/10	Update Wide temperature
1.7	2024/12	Revise 1.2 Features Update overview
1.8	2025/08	Update order information

1. Product Description

1.1 Overview

Silicon Power Computer & Communications industrial DRAM products are JEDEC standard 262-Pin low power Double Data Rate 5 (DDR5) Synchronous DRAM Small Outline Dual In-Line Memory Module (SODIMM). DDR5 SODIMM provide a high-performance, flexible 8-byte interface in a space-saving footprint. It is commonly used as the main memory in computers and other devices due to its cost-effectiveness and relatively high speed.

1.2 Features

- Fast data transfer rates:

Module Transfer Rates	Supported Transfer Rates	
	DDR5-4800(CL40)	DDR5-5600 (CL46)
DDR5-4800	V	
DDR5-5600	V	V

- Single or Dual rank
- V_{DD} = V_{DDQ} = 1.1V ±0.06V
- Terminated clock, control and command/address
- Halogen-free
- Data bus inversion (DBI) for data bus
- Integrated serial presence-detect (SPD) EEPROM
- Fly-by topology
- Gold edge contacts

2. Specification

2.1 Physical Dimension

2.1.1 Dimension

Table 1 : DRAM DDR5 SODIMM Physical Dimension

Parameter	Dimension
Length	69..60 ± 0.1mm
Width	30.0 ± 0.1mm
Thickness (connector)	1.2mm ± 0.1mm

2.1.2 Weight

- 9.5g ± 10%

2.2 Performance

- DDR5-4800(PC5-38400)
- DDR5-5600(PC5-44800)

2.3 Environmental Conditions

Table 2: Environmental Conditions

Feature	Operating	Storage
Temperature (Normal Grade)	-20°C to +95°C	-55°C to +110°C
Humidity	10% to 95% RH, non-condensing	
Vibration	20G (Peak-to-Peak), 80~2000 Hz	
Shock	1,500G, 0.5ms	

Notice:

- Vibration: Duration, 30 min x 3 axis.
- Shock: 1500G, 0.5msec, half-sine wave, 3 times in each direction, total = 18 times (6 directions).
- Temperature: The temperature reading is for the environment defined as Ta.

2.4 Compliance Specifications

- RoHS

3. Functional Description

3.1 Pin Assignment

Table 3: Pin Assignment

262-Pin DDR5 SODIMM Front								262-Pin DDR5 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BVLK	67	V_{SS}	131	CK0_A_t	197	V_{SS}	2	HSA	68	DQ21_A	132	CK1_A_t	198	DQ7_B
3	VIN_BVLK	69	DQ22_A	133	CK0_A_c	199	DQ8_B	4	HSCL	70	V_{SS}	134	CK1_A_c	200	V_{SS}
5	RFV	71	V_{SS}	135	V_{SS}	201	V_{SS}	6	HSDA	72	DQ23_A	136	V_{SS}	202	DQ9_B
7	PWR_GOOD	73	DQ24_A	137	CK0_B_t	203	DQ10_B	8	PWR_EN	74	V_{SS}	138	CK1_B_t	204	V_{SS}
9	V_{SS}	75	V_{SS}	139	CK0_B_c	205	V_{SS}	10	V_{SS}	76	DQ25_A	140	CK1_B_c	206	DQ11_B
11	DQ0_A	77	DQ26_A	141	V_{SS}	207	DQS1_B_c	12	DQ1_A	78	V_{SS}	142	V_{SS}	208	V_{SS}
13	V_{SS}	79	V_{SS}	143	RFV	209	DQS1_B_t	14	V_{SS}	80	DQ27_A	144	CA12_B	210	DM1_B_n
15	DQ2_A	81	DQS3_A_c	145	CA11_B	211	V_{SS}	16	DQ3_A	82	V_{SS}	146	CA10_B	212	V_{SS}
17	V_{SS}	83	DQS3_A_t	147	V_{SS}	213	DQ12_B	18	V_{SS}	84	DM3_A_n	148	V_{SS}	214	DQ13_B
19	DM0_A_n	85	V_{SS}	149	CA9_B	215	V_{SS}	20	DQS0_A_	86	V_{SS}	150	CA8_B	216	V_{SS}
21	V_{SS}	87	DQ28_A	151	CA7_B	217	DQ14_B	22	DQS0_A_	88	DQ29_A	152	CA6_B	218	DQ15_B
23	DQ4_A	89	V_{SS}	153	V_{SS}	219	V_{SS}	24	V_{SS}	90	V_{SS}	154	V_{SS}	220	V_{SS}
25	V_{SS}	91	DQ30_A	155	CA5_B	221	DQ16_B	26	DQ5_A	92	DQ31_A	156	CA4_B	222	DQ17_B
27	DQ6_A	93	V_{SS}	157	CA3_B	223	V_{SS}	28	V_{SS}	94	V_{SS}	158	CA2_B	224	V_{SS}
29	V_{SS}	95	CB0_A	159	V_{SS}	225	DQ18_B	30	DQ7_A	96	CB1_A	160	V_{SS}	226	DQ19_B
31	DQ8_A	97	V_{SS}	161	CS0_B_n	227	V_{SS}	32	V_{SS}	98	V_{SS}	162	CA1_B	228	V_{SS}
3	V_{SS}	99	CB2_A	16	RESET_n	22	DM2_B_n	3	DQ09_A	10	DQS4_A_	16	CA0_B	23	DQS2_B_

3				3		9		4		0	c	4		0	c
35	DQ10_A	101	V_{SS}	165	CS1_B_n	231	V_{SS}	36	V_{SS}	102	DQS4_A_t	166	V_{SS}	232	DQS2_B_t
37	V_{SS}	103	CB3_A	167	V_{SS}	233	DQ20_B	38	DQ11_A	104	V_{SS}	168	CB0_B	234	V_{SS}
39	DQS1_A_c	105	V_{SS}	169	DQS4_B_c	235	V_{SS}	40	V_{SS}	106	CS0_A_n	170	V_{SS}	236	DQ21_B
41	DQS1_A_t	107	CA0_A	171	DQS4_B_t	237	DQ22_B	42	DM1_A_n	108	ALERT_n	172	CB1_B	238	V_{SS}
43	V_{SS}	109	CA1_A	173	V_{SS}	239	V_{SS}	44	V_{SS}	110	CS1_A_n	174	V_{SS}	240	DQ23_B
45	DQ12_A	111	V_{SS}	175	CB3_B	241	DQ24_B	46	DQ13_A	112	V_{SS}	176	CB2_B	242	V_{SS}
47	V_{SS}	113	CA2_A	177	V_{SS}	243	V_{SS}	48	V_{SS}	114	CA3_A	178	V_{SS}	244	DQ25_B
49	DQ14_A	115	CA4_A	179	DQ0_B	245	DQ26_B	50	DQ15_A	116	CA5_A	180	DQ1_B	246	V_{SS}
51	V_{SS}	117	V_{SS}	181	V_{SS}	247	V_{SS}	52	V_{SS}	118	V_{SS}	182	V_{SS}	248	DQ27_B
53	DQ16_A	119	CA6_A	183	DQ2_B	249	DQS3_B_c	54	DQ17_A	120	CA7_A	184	DQ3_B	250	V_{SS}
55	V_{SS}	121	CA8_A	185	V_{SS}	251	DQS3_B_t	56	V_{SS}	122	CA9_A	186	V_{SS}	252	DM3_B_n
57	DQ18_A	123	V_{SS}	187	DM0_B_n	253	V_{SS}	58	DQ19_A	124	V_{SS}	188	DQS0_B_c	254	V_{SS}
59	V_{SS}	125	CA10_A	189	V_{SS}	255	DQ28_B	60	V_{SS}	126	CA11_A	190	DQS0_B_t	256	DQ29_B
61	DM2_A_n	KEY		191	DQ4_B	257	V_{SS}	62	DQS2_A_c	KEY		192	V_{SS}	258	V_{SS}
63	V_{SS}	127	CA12_A	193	V_{SS}	259	DQ30_B	64	DQS2_A_t	128	RFV	194	DQ5_B	260	DQ31_B
65	DQ20_A	129	V_{SS}	195	DQ6_B	261	V_{SS}	66	V_{SS}	130	V_{SS}	196	V_{SS}	262	V_{SS}

Notes: 1. On modules with nominal transfer rates <6400 MT/s, this pin is RFU. On modules with nominal transfer rates ≥6400 MT/s, this pin is NPP (no pin present).

3.2 Pin Description

Table 4 : Pin Description

Symbol	Type	I/O Level	Description
CK0_A_t, CK0_A_c, CK1_A_t, CK1_A_c, CK0_B_t, CK0_B_c, CK1_B_t, CK1_Bc,	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA12_A, CA0_B - CA12_B	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins mat not be interchanged between devices on the same bus.
CS0_A_n - CS1_A_n, CS0_B_n - CS1_B_n	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks.
DQ0_A - DQ31_A, DQ0_B - DQ31_B	Input/ Output	VDDQ	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
CB0_A - CB3_A, CB0_B - CB3_B	Input/ Output	VDDQ	DIMM ECC check bits
DQS0_A_t - DQS4_A_t DQS0_A_c - DQS4_A_c DQS0_B_t - DQS4_B_t DQS0_B_c - DQS4_B_c	Input/ Output	VDDQ	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single- ended.

Symbol	Type	I/O Level	Description
DM0_A_n-DM3_A_, DM0_B_n-DM3_B_n	Input	VDDQ	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. .
ALERT_n	Input/ Output	VDD	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin mVst be bounded to VDDQ on board.
RESET_n	Input	VDD	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n mVst be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,
HSCL	Input	1.0V	Host SidebandBus bus clock, supplied by the controller.
HSDA	Input/ Output	1.0V	Host SidebandBus data, connected from the controller to Hub or Host bus Target devices.
HSA	Input	2.1V max	Host SidebandBus bus device ID address pin; input to a hub or other client device to distinguish between identical devices in the I3C-Basic/I2C address range.
RFV			Reserved for Future use. No on DIMM electrical connection is present.

Symbol	Type	I/O Level	Description
PWR_GOOD	Input/ Output	Open Drain	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or configured in the appropriate

			register or and LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
PWR_EN	Input	3.3V	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. this signal is connected to PMIC's VR_EN pin.
VIN_BVLK	Supply	5V	5V power input supply to the PMIC for analog circuits.
VSS	Supply		Ground

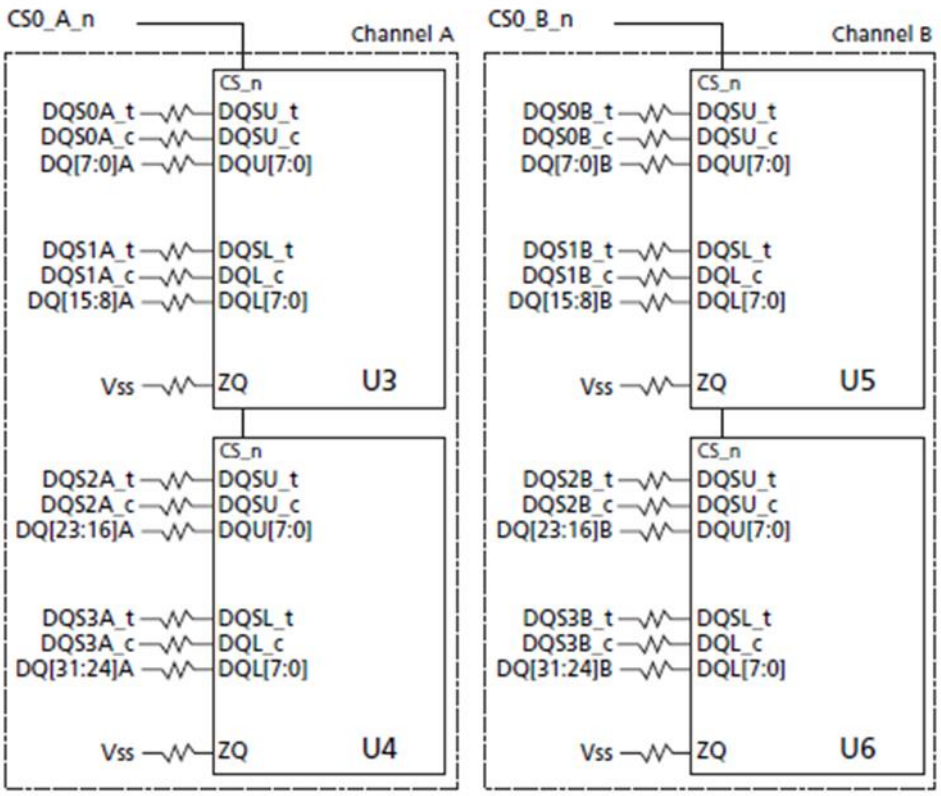
3.3 Absolute Maximum DC Ratings

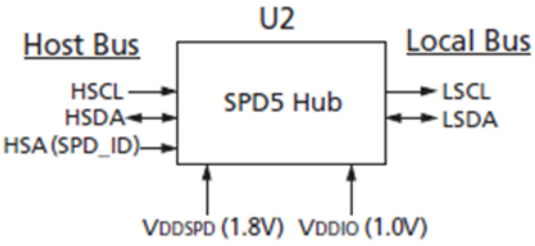
Table 5: Absolute Maximum DC Ratings

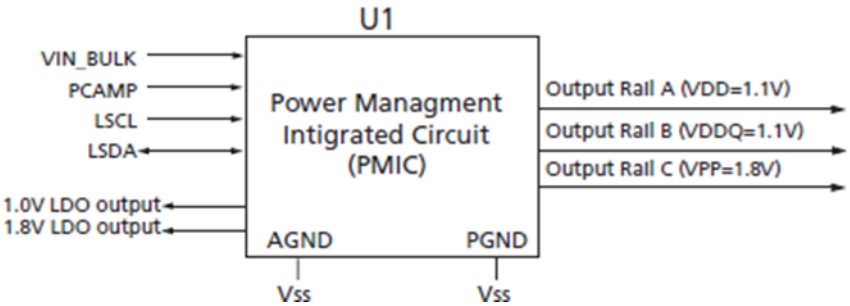
Symbol	Parameter	Rating	Units
V_{DDSPD}	Storage temperature	-65 ~ 150	℃
V_{DDIO}	Supply voltage	-0.5 ~ 2.1	V
V_{DDSPD}	Supply voltage	-0.5 ~ 2.1	V
HSA	HSA pin	-0.5 ~ 2.1	V
HSCL, HSDA, LSCL, LSDA	HSCL, HSDA, LSCL, LSDA pins	-0.5 ~ 3.6	V

4. Block Diagram & Simplified Mechanical Drawing

4.1 Block Diagram(x16 1Rank without ECC)





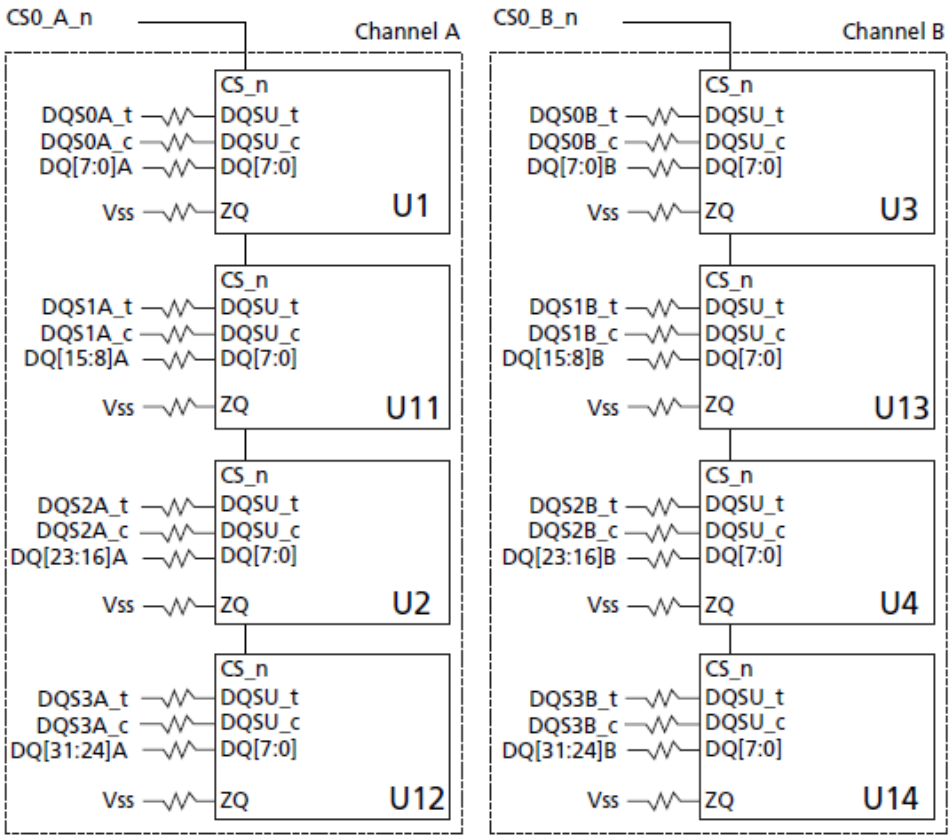


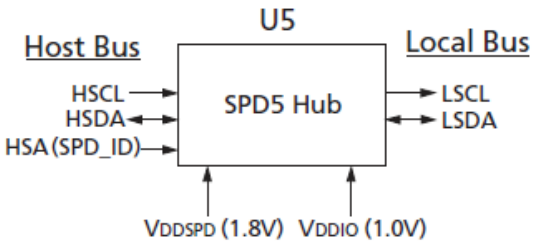
Notes:

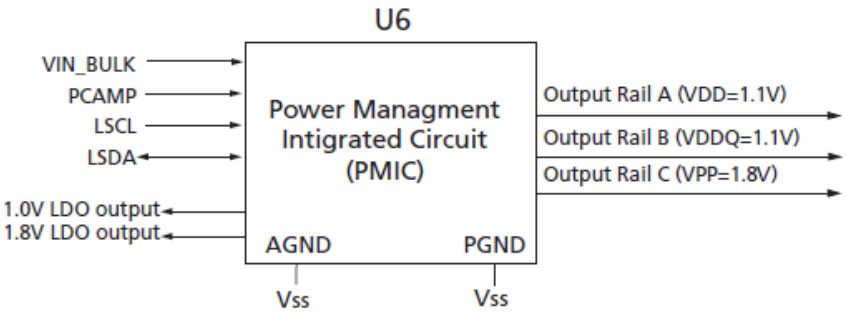
1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

2. Functional block diagram is for reference only.

4.2 Block Diagram(x8 1Ranks without ECC)



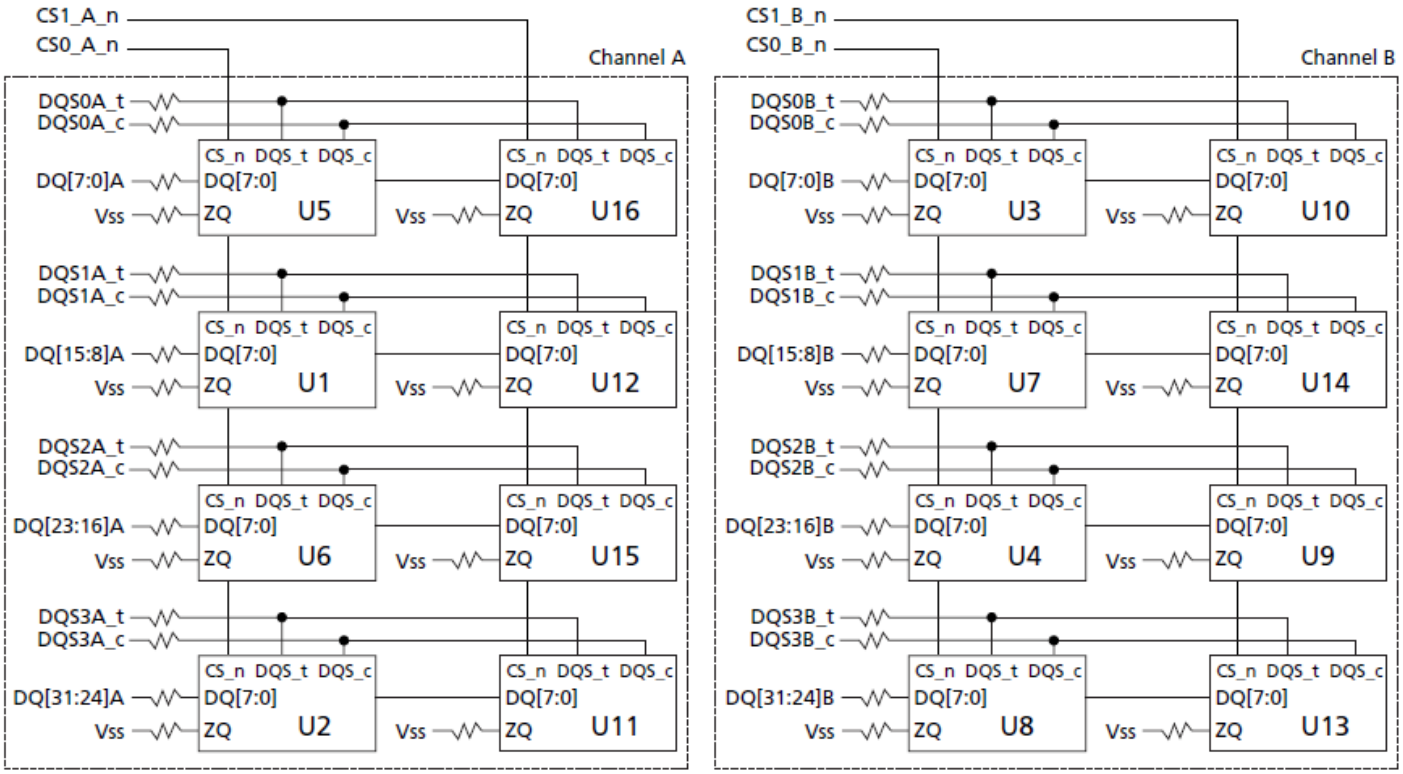


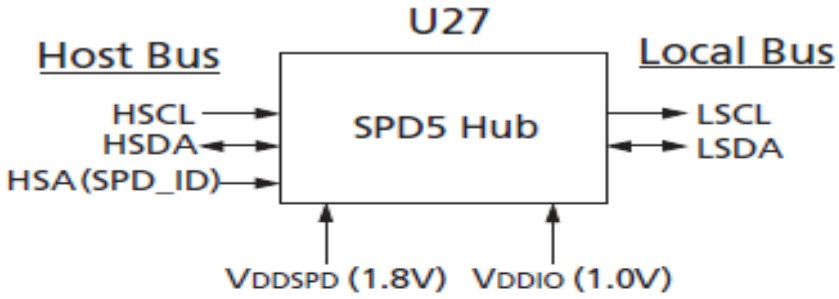


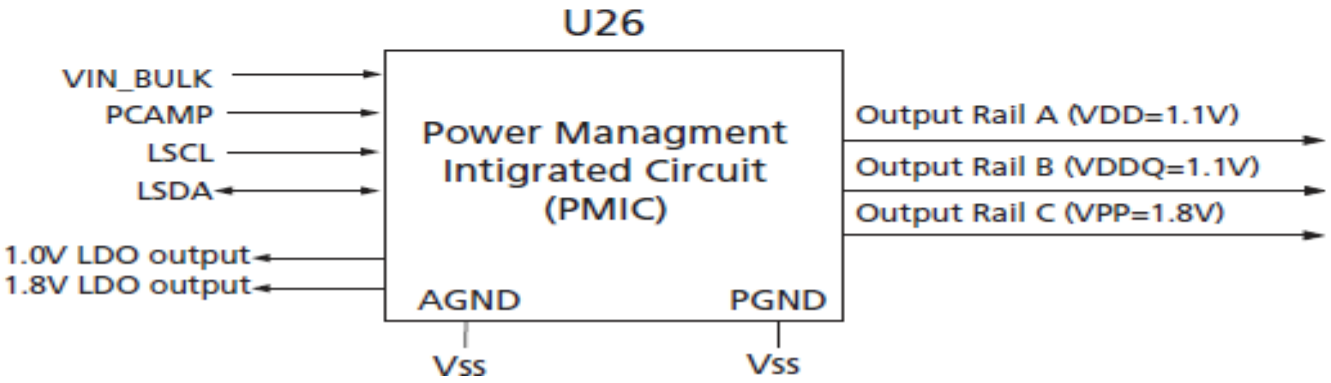
Notes:

1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to groVnd. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

4.3 Block Diagram(x8 2Ranks without ECC)



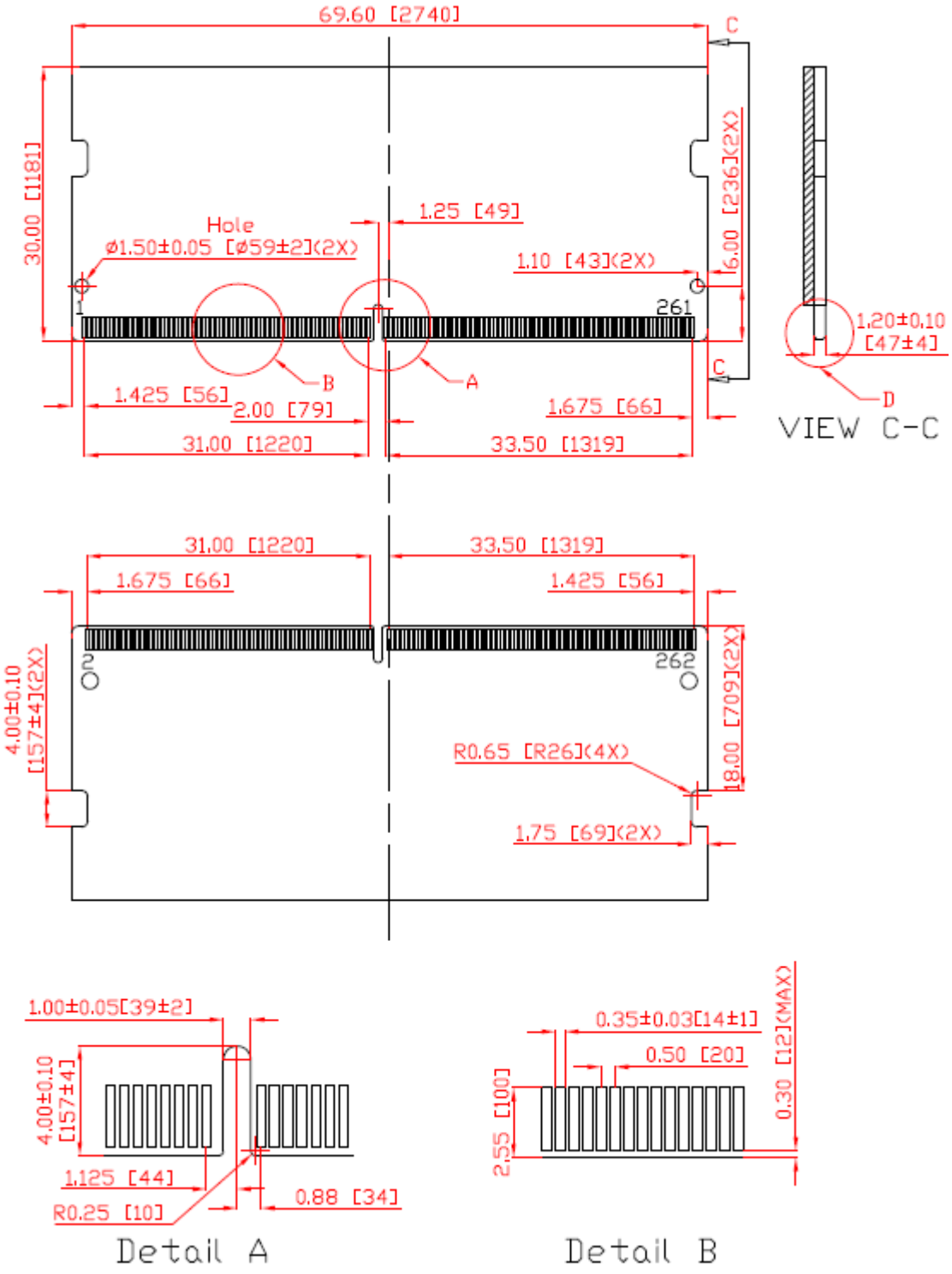




Notes: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

2. Functional block diagram is for reference only.

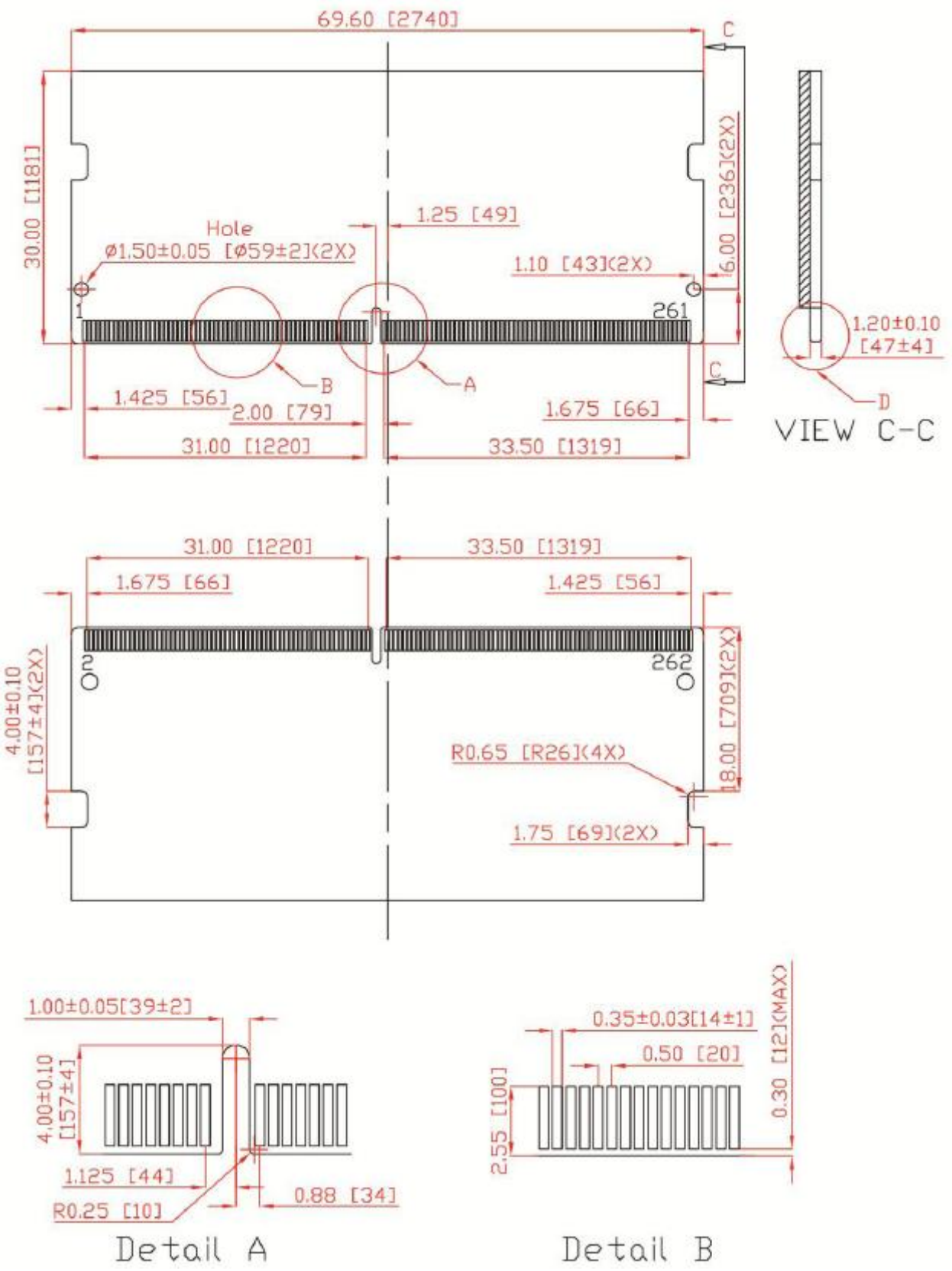
4.4 Simplified Mechanical Drawing (64bits SODIMM x16 1Rank)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Notes: 2. The dimensional diagram is for reference only.

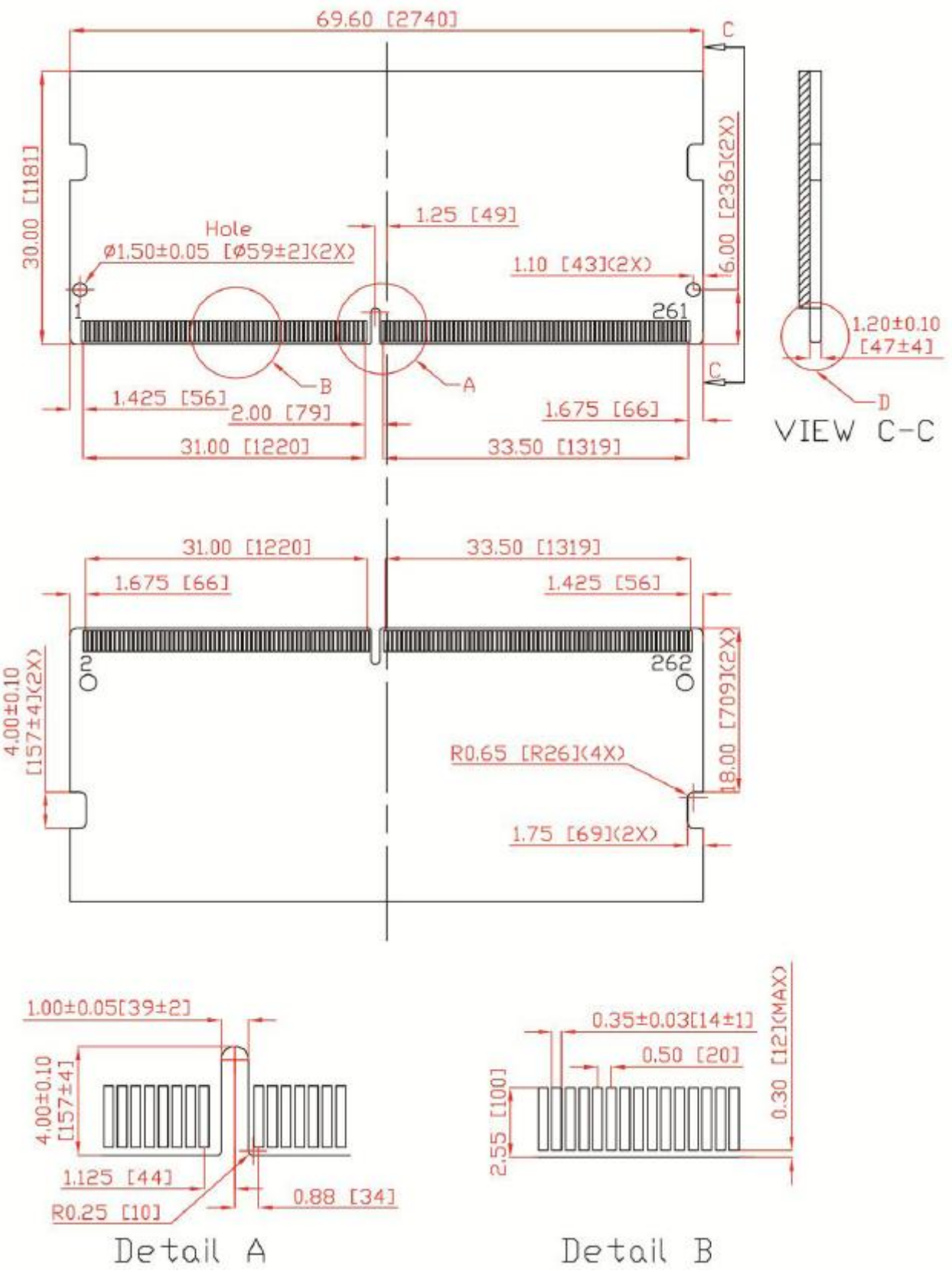
4.5 Simplified Mechanical Drawing (64bits SODIMM x8 1Rank)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Notes: 2. The dimensional diagram is for reference only.

4.6 Simplified Mechanical Drawing (64bits SODIMM x8 2Ranks)



5. Ordering Information

5.1 Part Number Definition

Table 6 : Part Number Definition

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	S	P	0	4	8	G	I	S	V	U	5	6	0	P	H	0

Code 1-2: Brand	SP: Silicon Power
Code 3-6: Capacity	008G: 8GB: 016G: 16GB ; 032G: 32GB; 048G: 48GB
Code 7: Product	I: Industrial Grade Product
Code 8-9: Type & Form Factor	S:SODIMM; V:DDR5
Code 10: Operation Temperature	U: Normal Temperature -20°C to +95°C V: Wide Temperature -40°C to +105°C
Code 11-13: Model Series	480:4800; 560: 5600
Code 14: Chip Specification	F: 2Gx8 G: 1Gx16 P: 3Gx8
Code 15: Chip Brand	H: Hynix; N: Nanya
Code 16: Reserved	0: Standard
Code 17-18	For customization

5.2 Standard DDR5 SODIMM 4800 Series Information

Capacity	Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing
Normal Temperature (-20°C ~ 95°C)					
8GB	SP008GISVU480GH0	8GB (1Gbx64) 1Gx16, 1Rank	38.4GB/s	DDR5-4800	40-39-39
16GB	SP016GISVU480FH0	16GB (2Gbx64) 2Gx8, 1Rank	38.4GB/s	DDR5-4800	40-39-39
32GB	SP032GISVU480FH0	32GB (4Gbx64) 2Gx8, 2Ranks	38.4GB/s	DDR5-4800	40-39-39

5.3 Standard DDR5 SODIMM 5600 Series Information

Capacity	Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing
Normal Temperature (-20°C ~ 95°C)					
8GB	SP008GISVU560GH0	8GB (1Gbx64) 1Gx16, 1Rank	44.8GB/s	DDR5-5600	46-45-45
8GB	SP008GISVU560GN0	8GB (1Gbx64) 1Gx16, 1Rank	44.8GB/s	DDR5-5600	46-45-45
16GB	SP016GISVU560FH0	16GB (2Gbx64) 2Gx8, 1Rank	44.8GB/s	DDR5-5600	46-45-45
32GB	SP032GISVU560FH0	32GB (4Gbx64) 2Gx8, 2Ranks	44.8GB/s	DDR5-5600	46-45-45
48GB	SP048GISVU560PH0	48GB (6Gbx64) 3Gx8, 2Ranks	44.8GB/s	DDR5-5600	46-45-45
Wide Temperature (-40°C ~ 105°C)					
8GB	SP008GISVV560GH0	8GB (1Gbx64) 1Gx16, 1Rank	44.8GB/s	DDR5-5600	46-45-45
8GB	SP008GISVV560GN0	8GB (1Gbx64) 1Gx16, 1Rank	44.8GB/s	DDR5-5600	46-45-45
16GB	SP016GISVV560FH0	16GB (2Gbx64) 2Gx8, 1Rank	44.8GB/s	DDR5-5600	46-45-45
32GB	SP032GISVV560FH0	32GB (4Gbx64) 2Gx8, 2Ranks	44.8GB/s	DDR5-5600	46-45-45
48GB	SP048GISVV560PH0	48GB (6Gbx64) 3Gx8, 2Ranks	44.8GB/s	DDR5-5600	46-45-45

5.4 Appendix

Table 7 : Abbreviation

Item	Abbreviation	Description
1	MTBF	Mean Time Between Failures
2	ECC	Error Correction Code
3	TCG	Trusted Computing Group
4	AES	Advanced Encryption Standard
5	OP	Over Provisioning
6	PS	Power Shield
7	DC	Direct Current
8	DRAM	Dynamic Random Access Memory
9	WAF	Write Amplification Factor
10	WLE	Wear Leveling Efficiency
11	Ta	Ambient Temperature
12	LBA	Logical Block Address

Contact Information

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